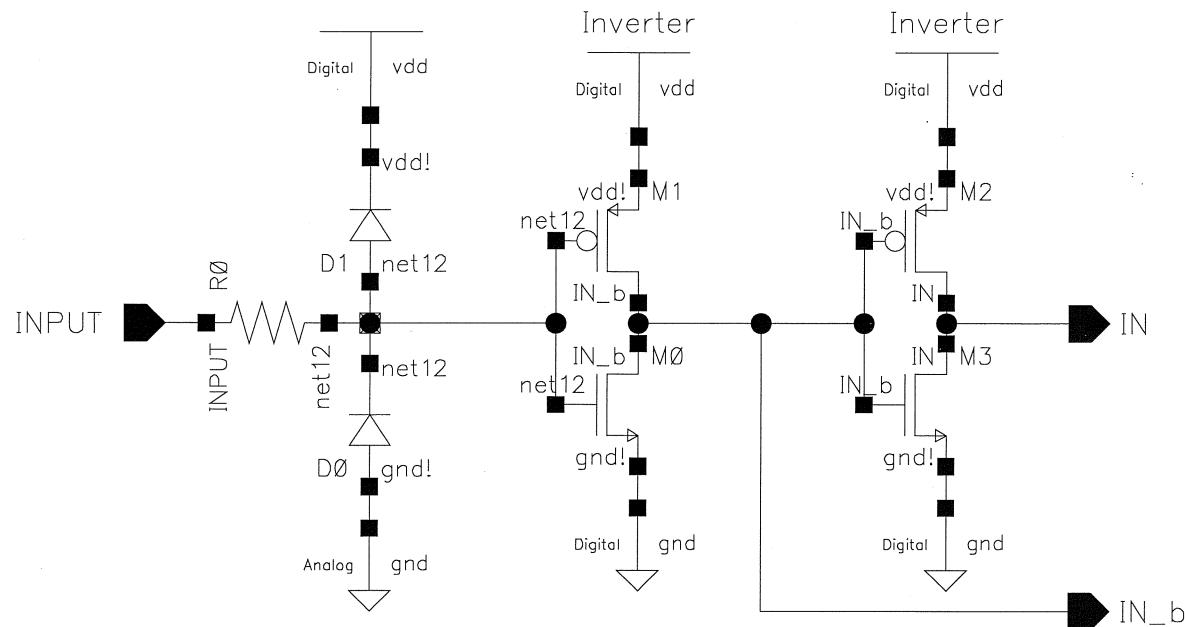


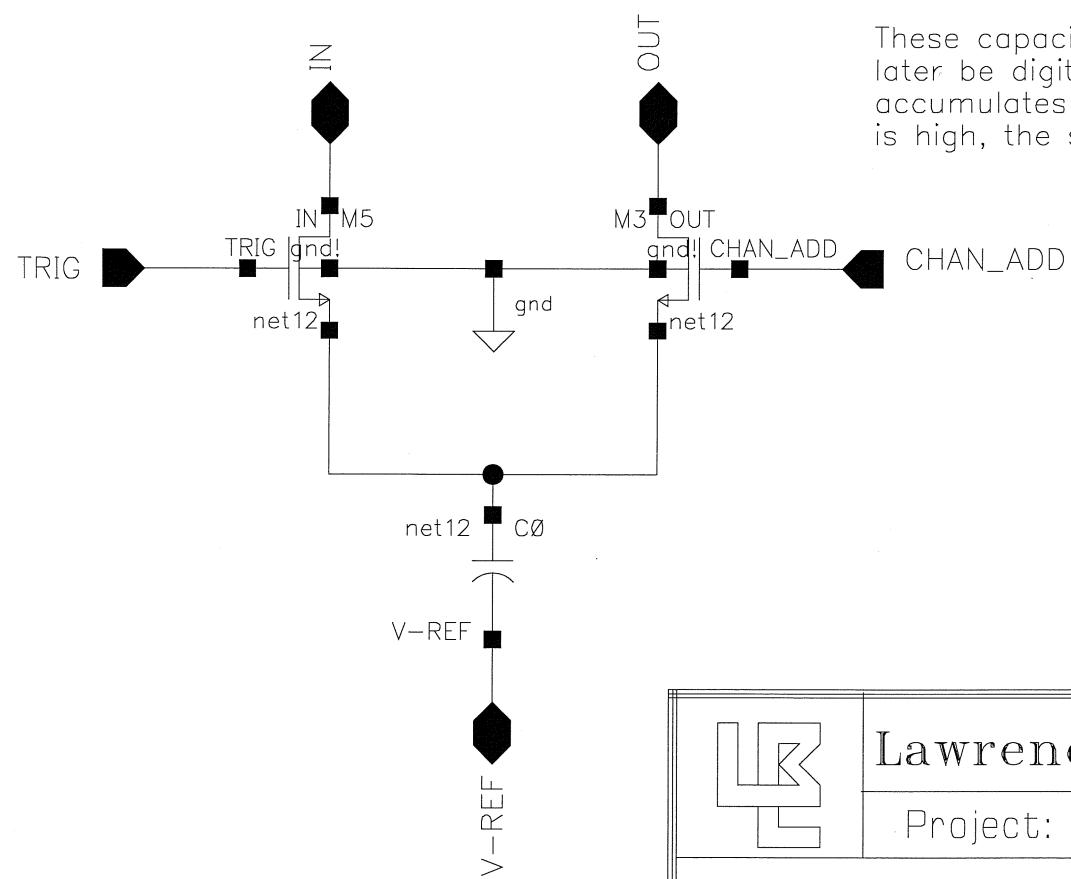
 Lawrence Berkeley National Lab
 Project: Analog Transient Waveform Digitizer
 Library: OATWD
 CellName: ATWD
 UPDATE: Sep 28 16:45:21 1999 Size: B
 DESIGN: oren Sheet of 1



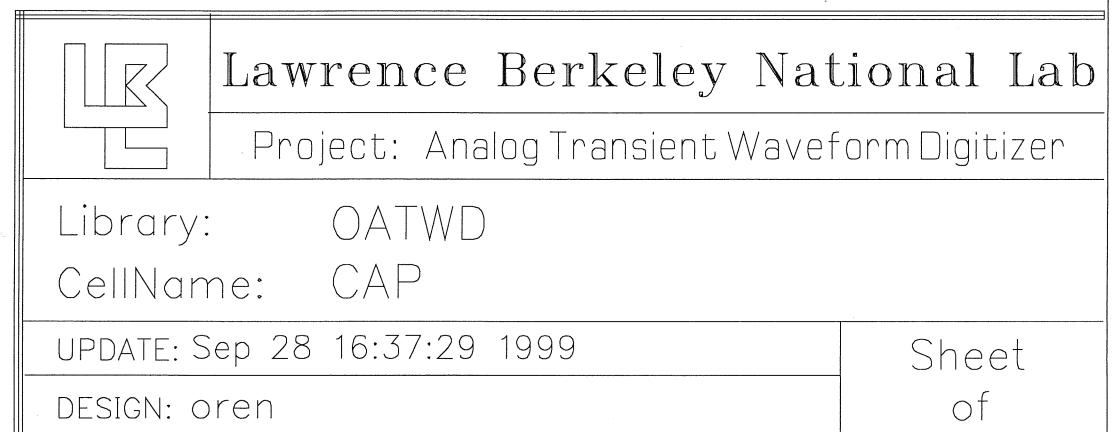
These digital inputs are protected by back biased diodes to the digital Vdd and to the analog gnd (I don't know if this was a design consideration). None of the protective diodes are robust in nature, so ESD suppression precautions must be taken while handling the device. The value of the resistance and the diodes could not be extracted from the layout.

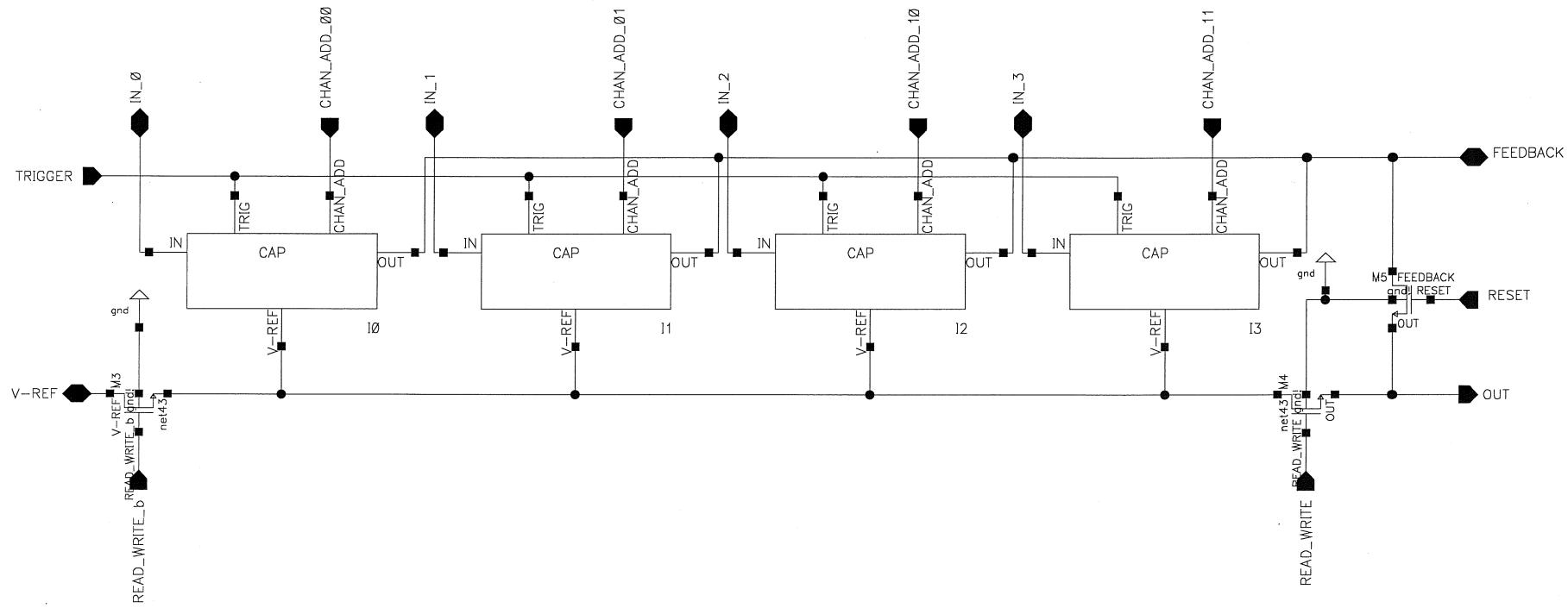
INPUT parameters:
 Minimum HIGH = 2.7 V. Typical HIGH > 3 V.
 Maximum LOW = 2 V. Typical LOW < 1 V.

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Library:	OATWD
CellName:	IN
UPDATE:	Sep 28 16:37:31 1999
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These capacitors are used to store a charge that will later be digitized. When TRIG is high, charge accumulates on the capacitor. When the CHAN_ADD is high, the signal goes to the OP_AMP



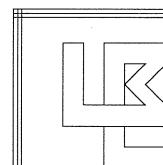
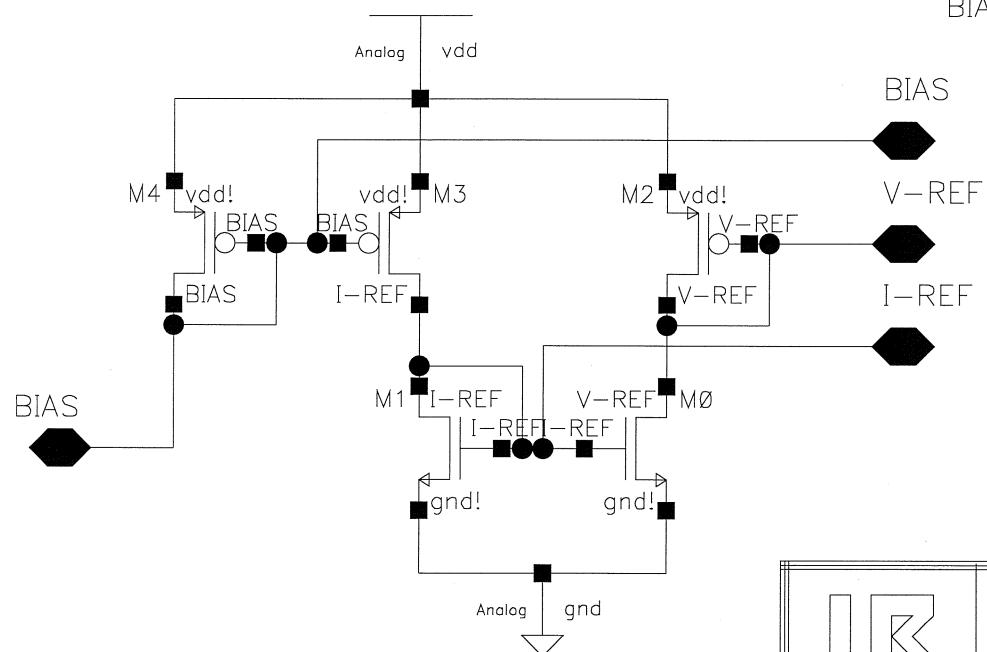


This circuit holds the value of four different inputs. To store a charge, the TRIGGER and READ_WRITE_b must be high. It is also a good idea to have RESET high to reset the OP-AMP. This charge is then digitized when the READ_WRITE and one of the CHAN_ADD is high. NOTE: ANALOG_RESET must be low to digitize. The CHAN_ADD controls which channel.

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Library:	OATWD
CellName:	CAPS
UPDATE:	Sep 28 16:37:30 1999
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This is the bias for the comparator. Note that the off-chip BIAS is directly attached to the BIAS that goes to the comparator. I used a 100k ohm resistor from BIAS to gnd to run my test, which had a value of 38.87u A.

BIAS: min = 20u A. max = 1m A. typ = 30–500u A.



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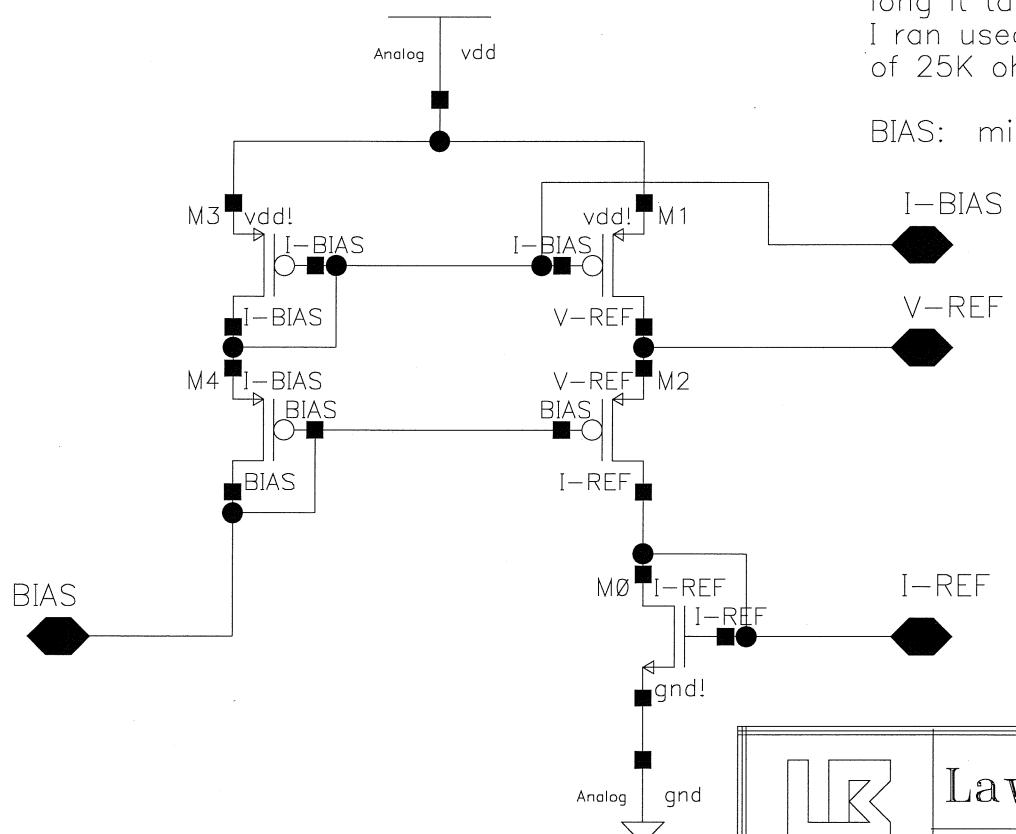
Library: OATWD

CellName: BIAS_Comp

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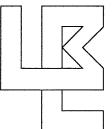
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This is the bias for the Op-Amp. The BIAS is an off-chip power supply. The lower the BIAS, the long it takes for the Op-Amp to settle. The test I ran used a resistor from BIAS to gnd with a value of 25K ohms, and a measured current of 71.1u A.

BIAS: min = 10u A. max = 400u A. typ = 40–120u A.

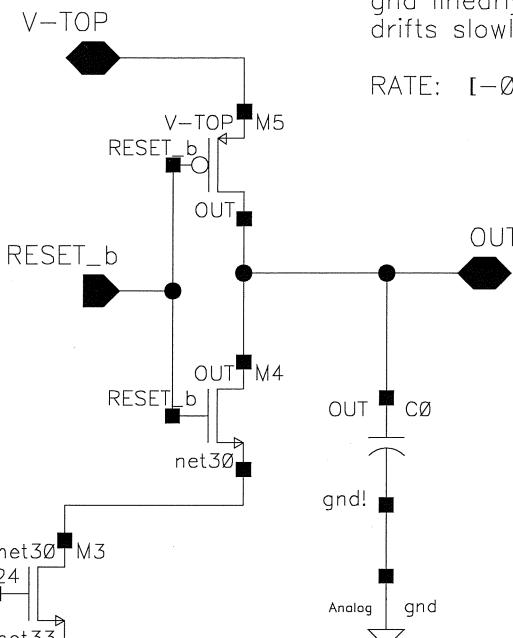
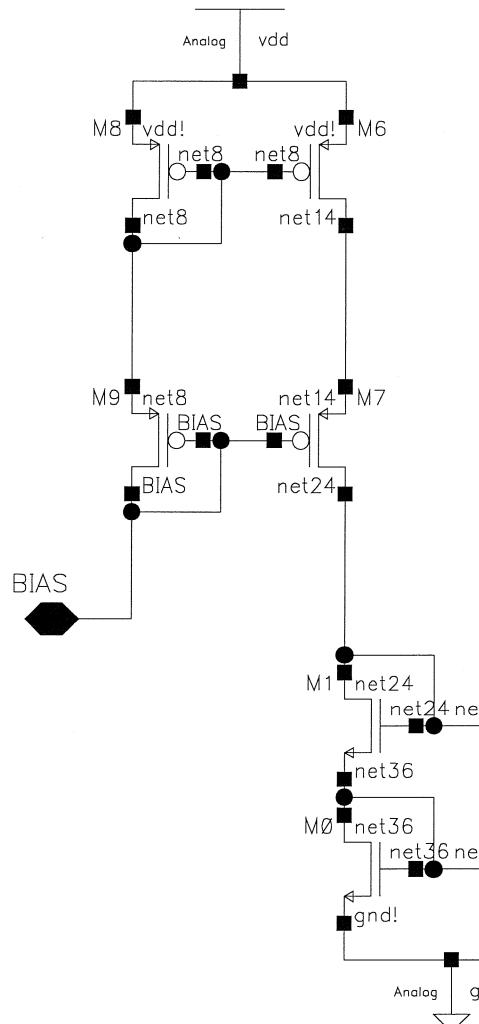

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Library:	OATWD
CellName:	BIAS_Op_Amp

UPDATE: Sep 28 16:37:27 1999

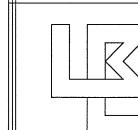
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This is a Voltage ramp for the ADC processes. Its top voltage is set by the V_TOP, and the slope of the ramp is set by the BIAS. The higher the ramp current, the steeper the slope. The RESET restarts the ramp at the top. The ramp goes from V_TOP to gnd linearly until it gets to about 0.2 V, and then drifts slowly to gnd. V_TOP has a maximum of 5.6 V.

RATE: [-0.006 * RAMP_BIAS(in u A)] V per 10u S.



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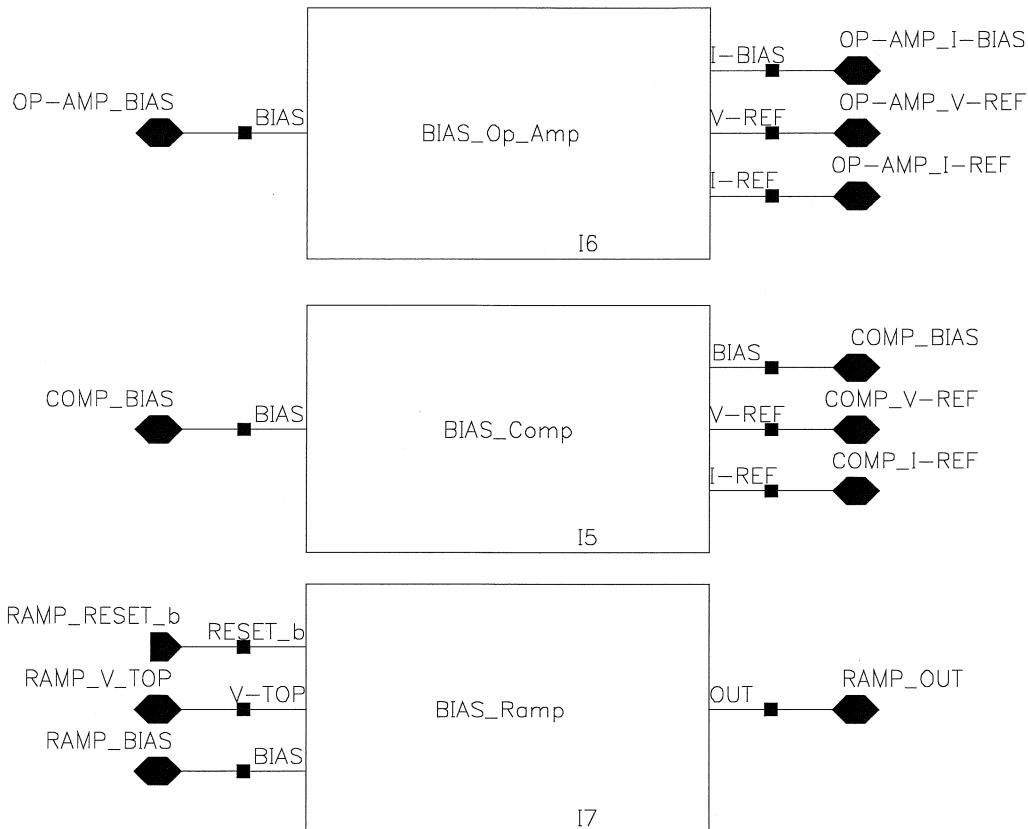
Library: OATWD

CellName: BIAS_Ramp

UPDATE: Sep 28 16:37:27 1999

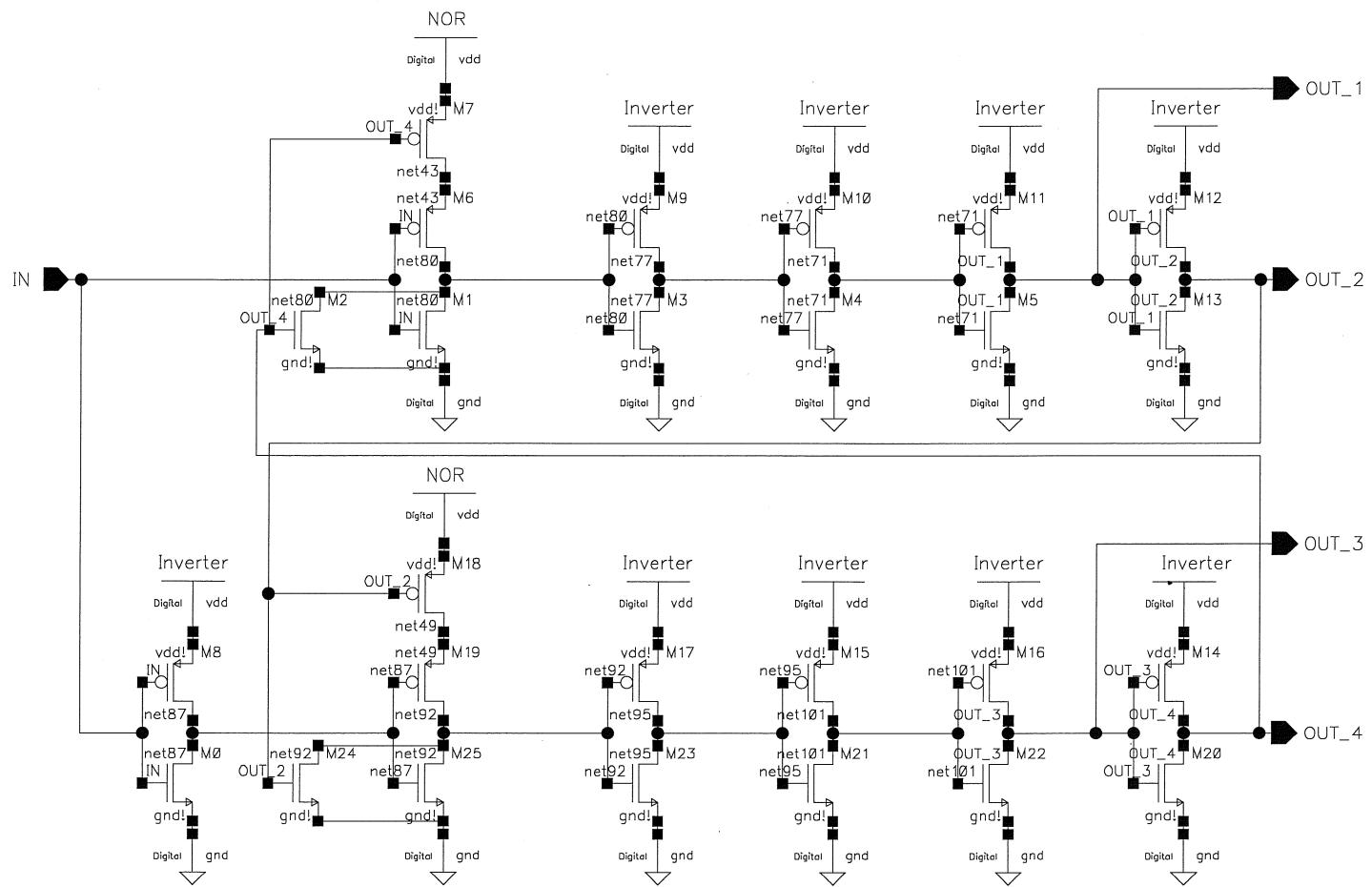
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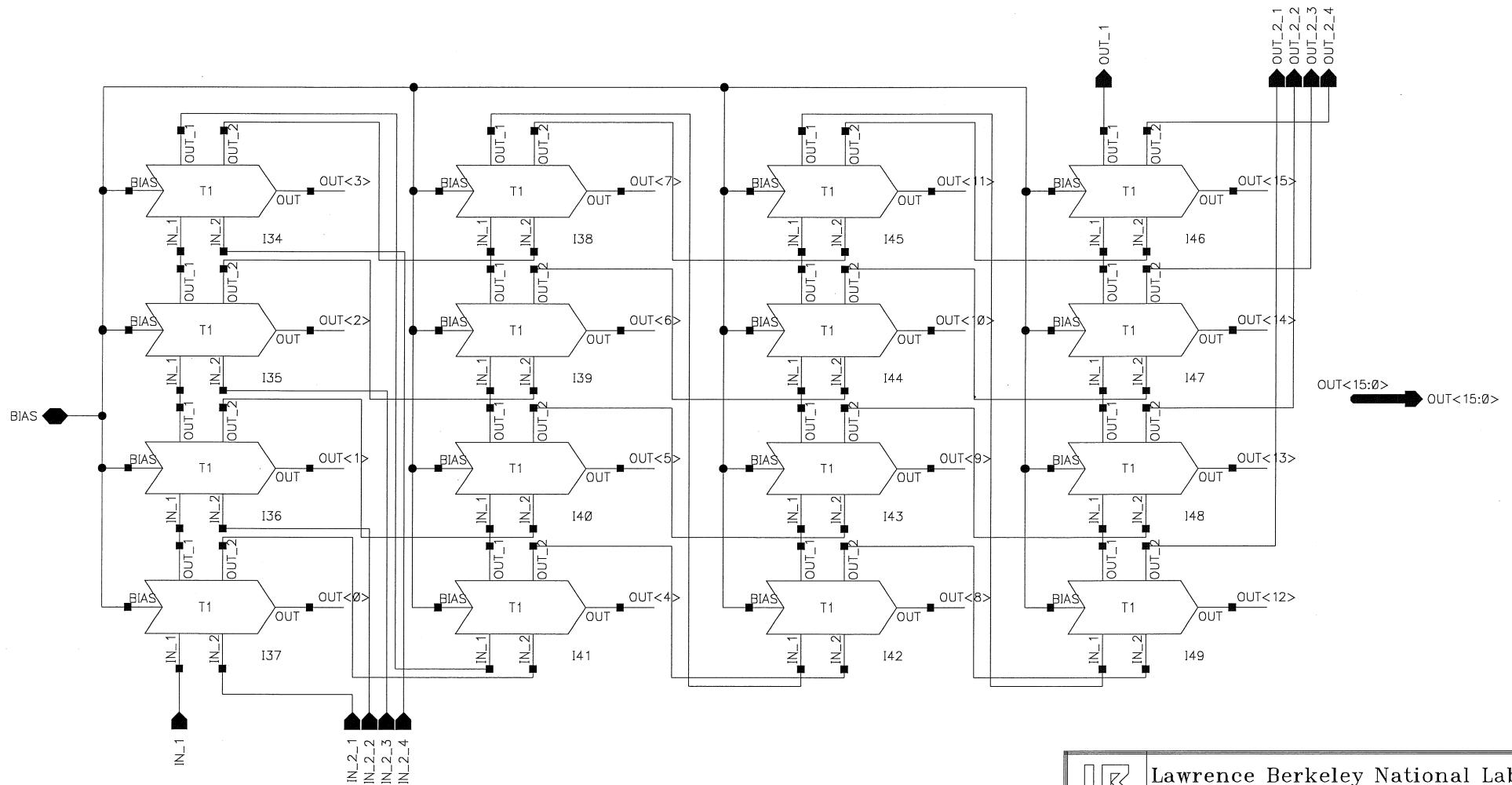
This circuit is the bias for the OP-AMP and the COMPARATOR. It also has the Ramp used for digitization. The off-chip sources are the OP-AMP_BIAS, COMP_BIAS, RAMP_V_TOP, and RAMP_BIAS. RAMP_RESET is a switch for resetting the RAMP.

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	Project: Analog Transient Waveform Digitizer
Library:	OATWD
CellName:	BIAS
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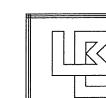


This clock controls the rate which the bits are shifted out of the slices.

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	Project: Analog Transient Waveform Digitizer
Library:	OATWD
CellName:	SHIFT_CLOCK
UPDATE:	Sep 28 16:37:26 1999
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The T16 is simply 16 T7's grouped together. Every fourth OUT_2 is connected to the IN_2.



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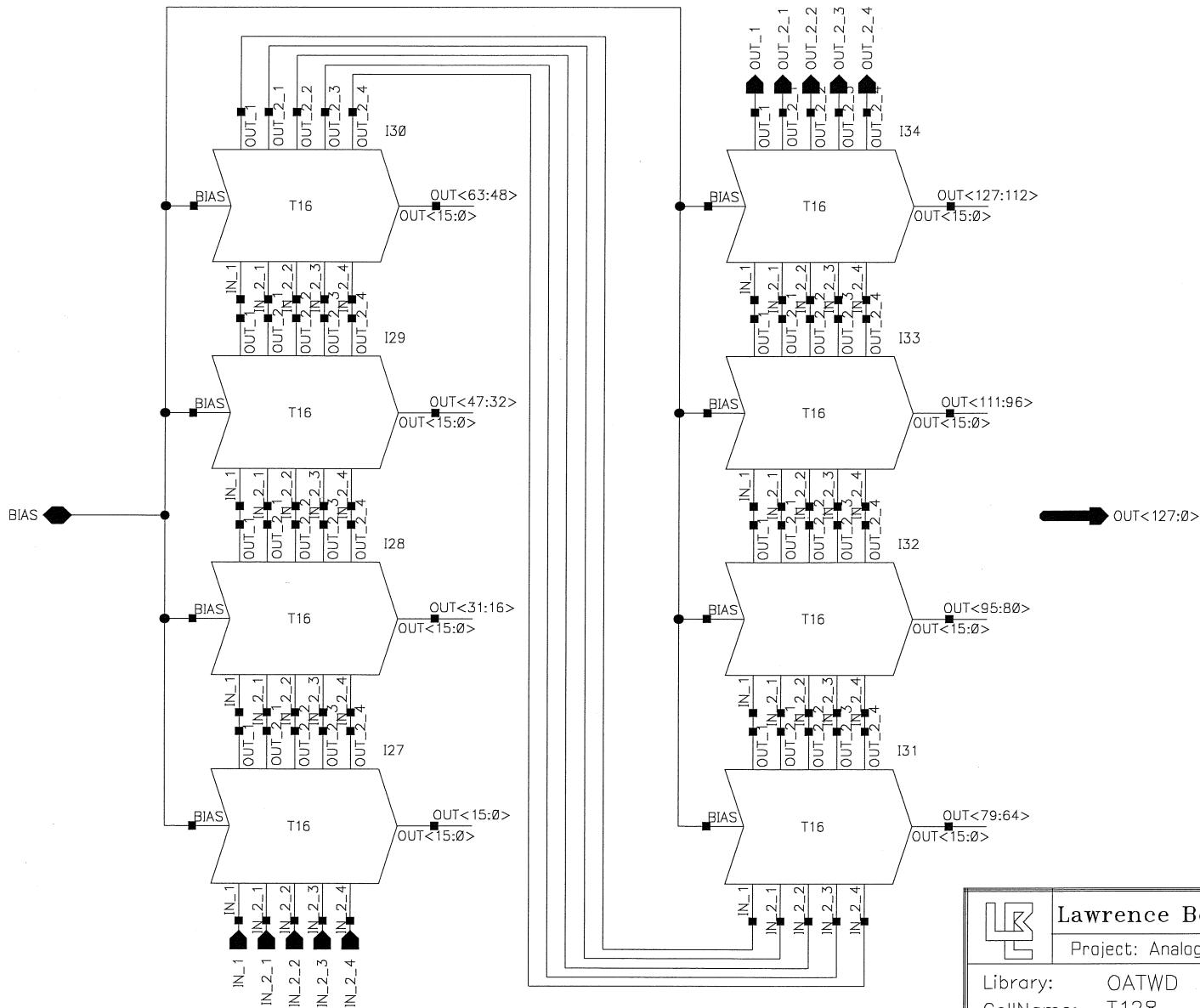
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CellName: T16

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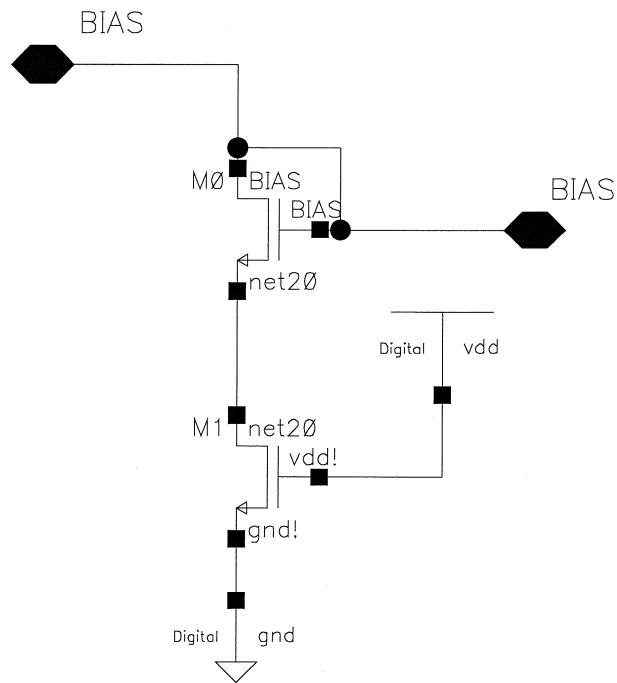
Project: Analog Transient Waveform Digitizer

Library: OATWD
CellName: T128

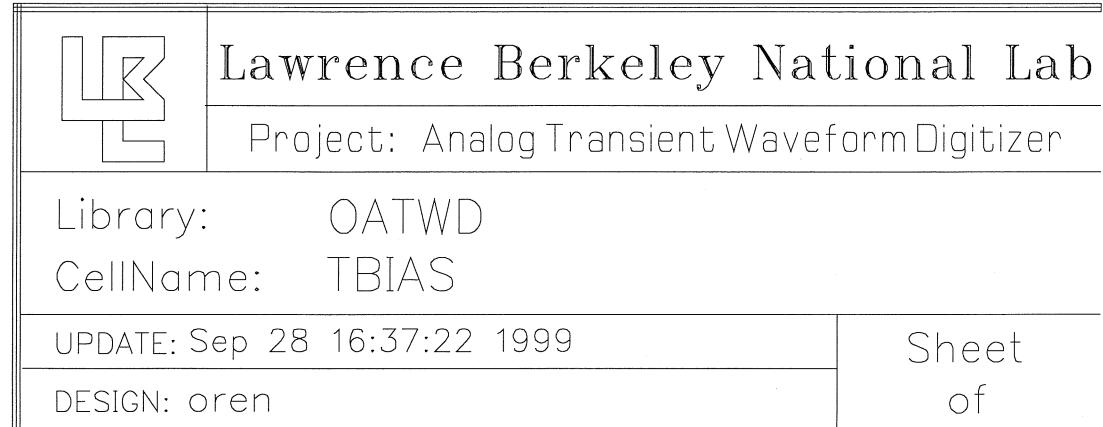
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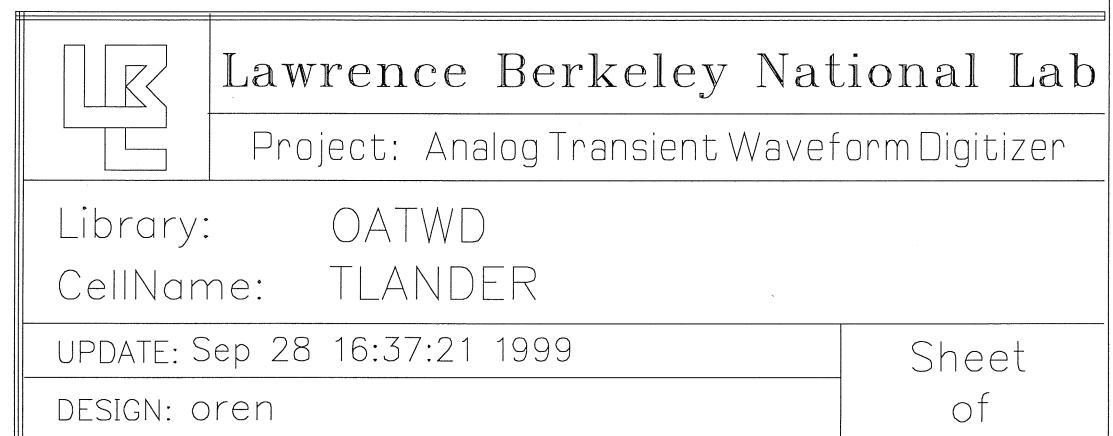
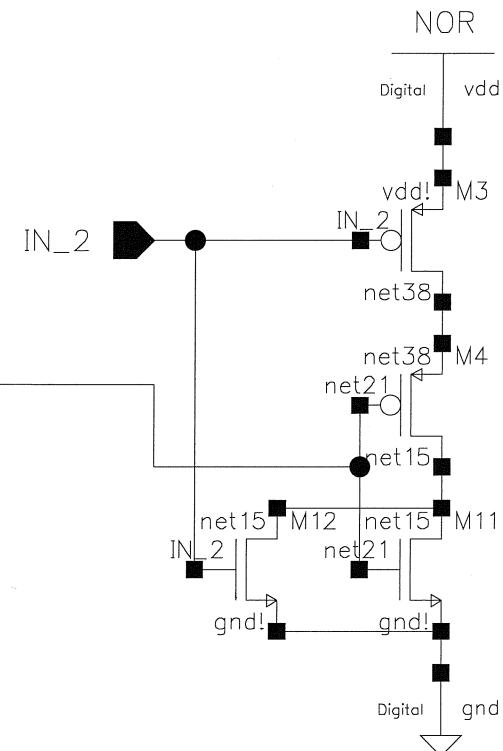
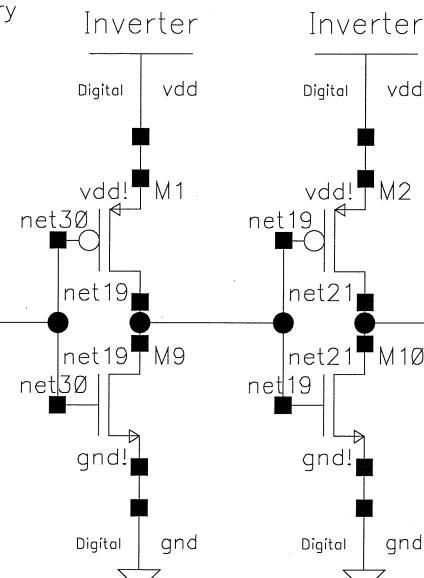
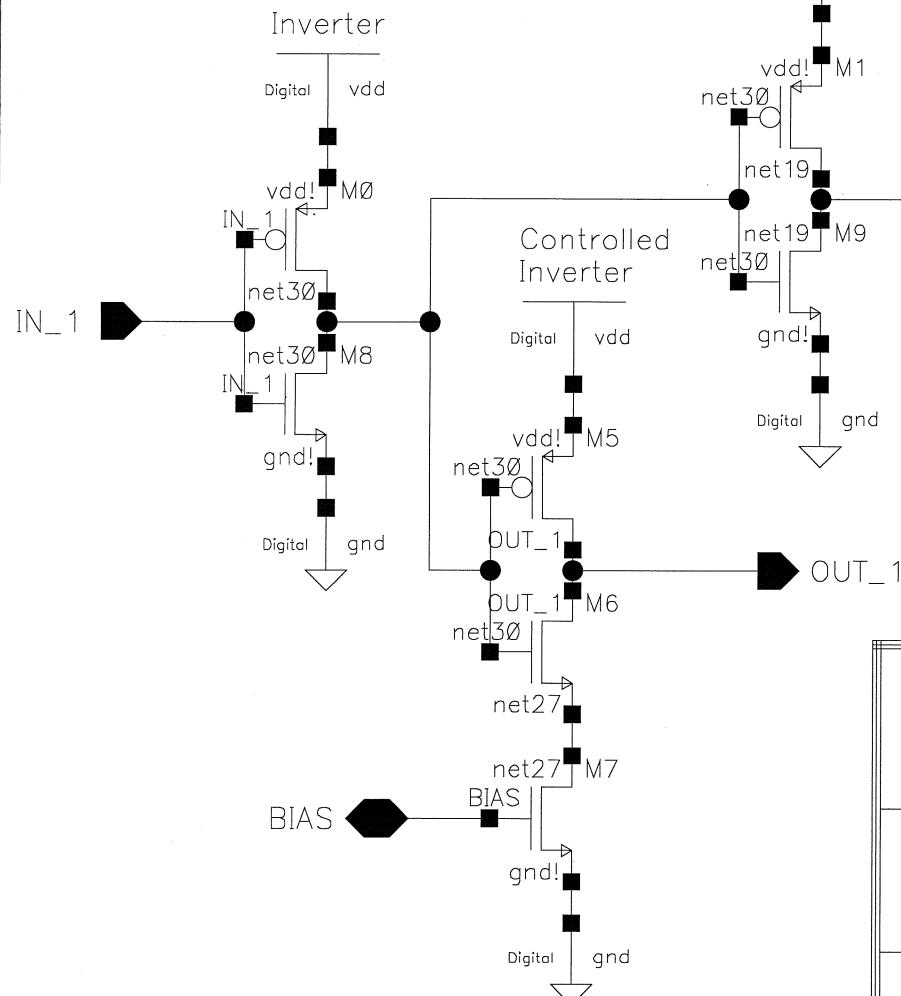
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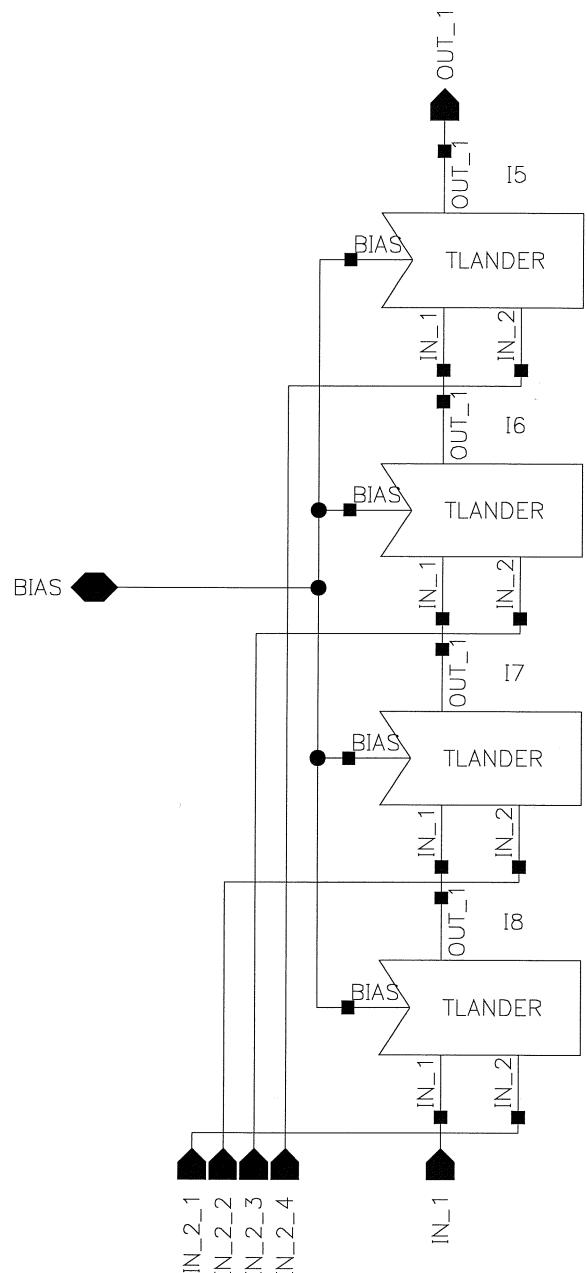


This is the bias for the Trigger.



The lander is a bogus T7. It has no output. What it does is continues the propagation after all 128 gates have been open. The reason is because every fourth out2 is connected, and to give the last four T7's the same impedance, the gates must be connected to dummy T7's.

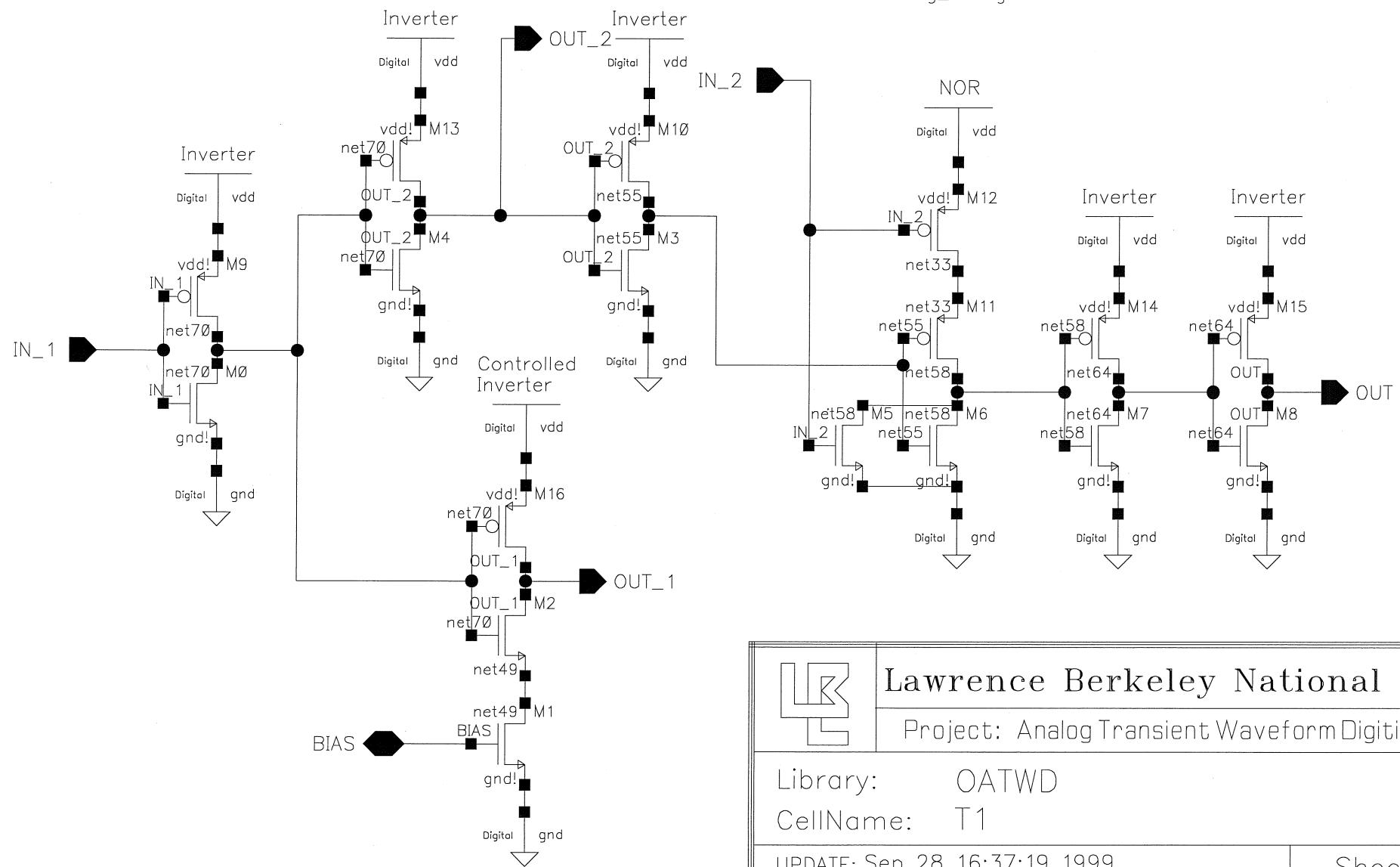




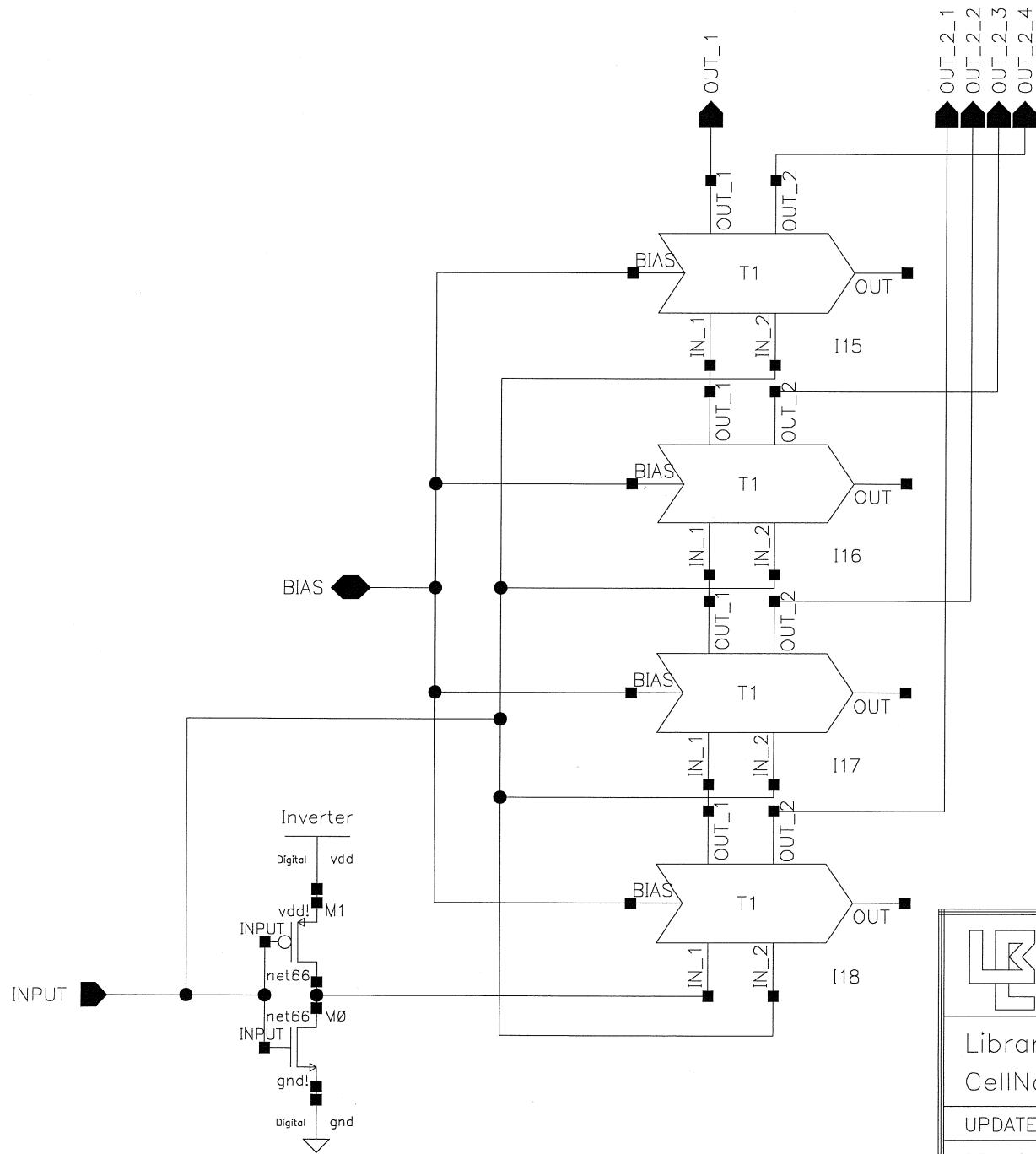
The TFINISH is four TLANDERS. This circuit 'lands' the signal so that the propagation remains smooth thought the TRIGGER circuit.

	Lawrence Berkeley National Lab
	Project: Analog Transient Waveform Digitizer
Library:	OATWD
CellName:	TFINISH
UPDATE:	Sep 28 16:37:22 1999
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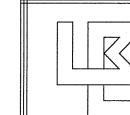
This is the basic building block of the trigger. Its speed is controlled by a controlled inverter. This controlled inverter sets the rate at which the propagation proceeds down the trigger. The OUT controls a gate that opens a storage capacitor to the Analog_In signal.



	Lawrence Berkeley National Lab
	Project: Analog Transient Waveform Digitizer
Library:	OATWD
CellName:	T1
UPDATE:	Sep 28 16:37:19 1999
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The TSTART circuit starts the propagation of the wave down the trigger. It is four T7's connected with their OUT2's going to the first four IN2 of the T128 block. The outputs are just hanging without any connections to simulate the same impedance values.



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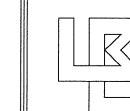
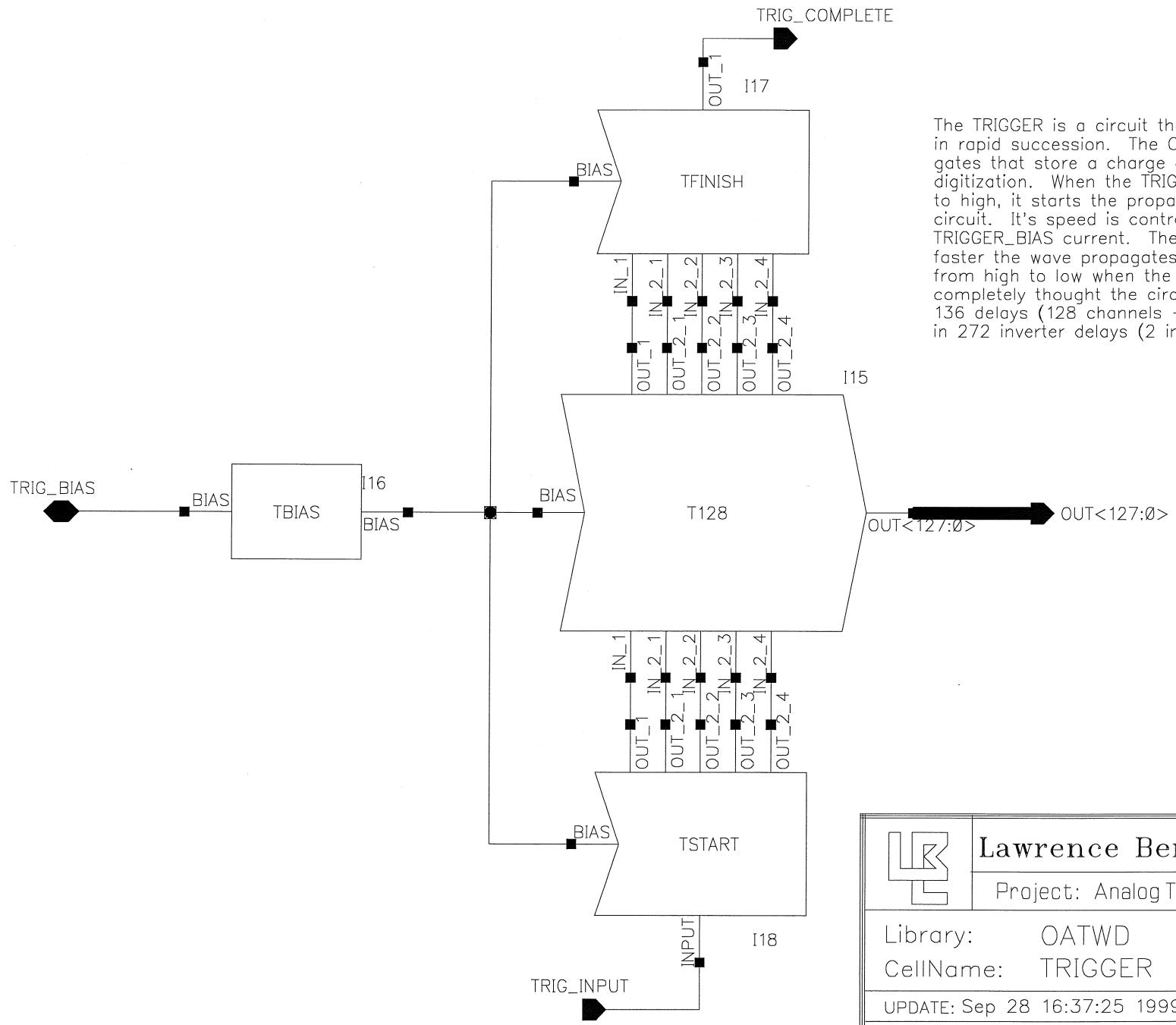
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CellName: TSTART

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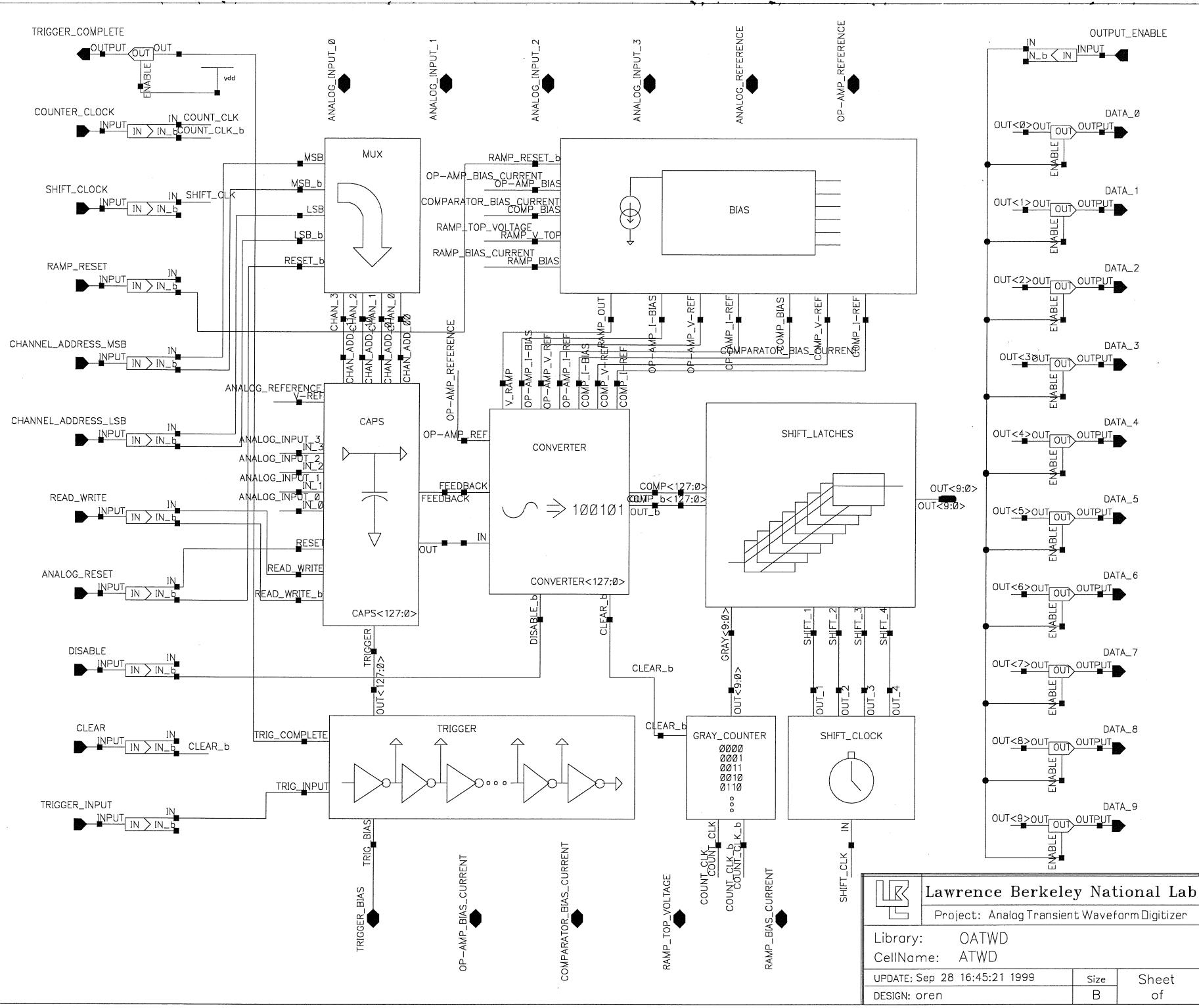
Library: OATWD

CellName: TRIGGER

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Library: OATWD

CellName: ATWD

UPDATE: Sep 28 16:45:21 1999

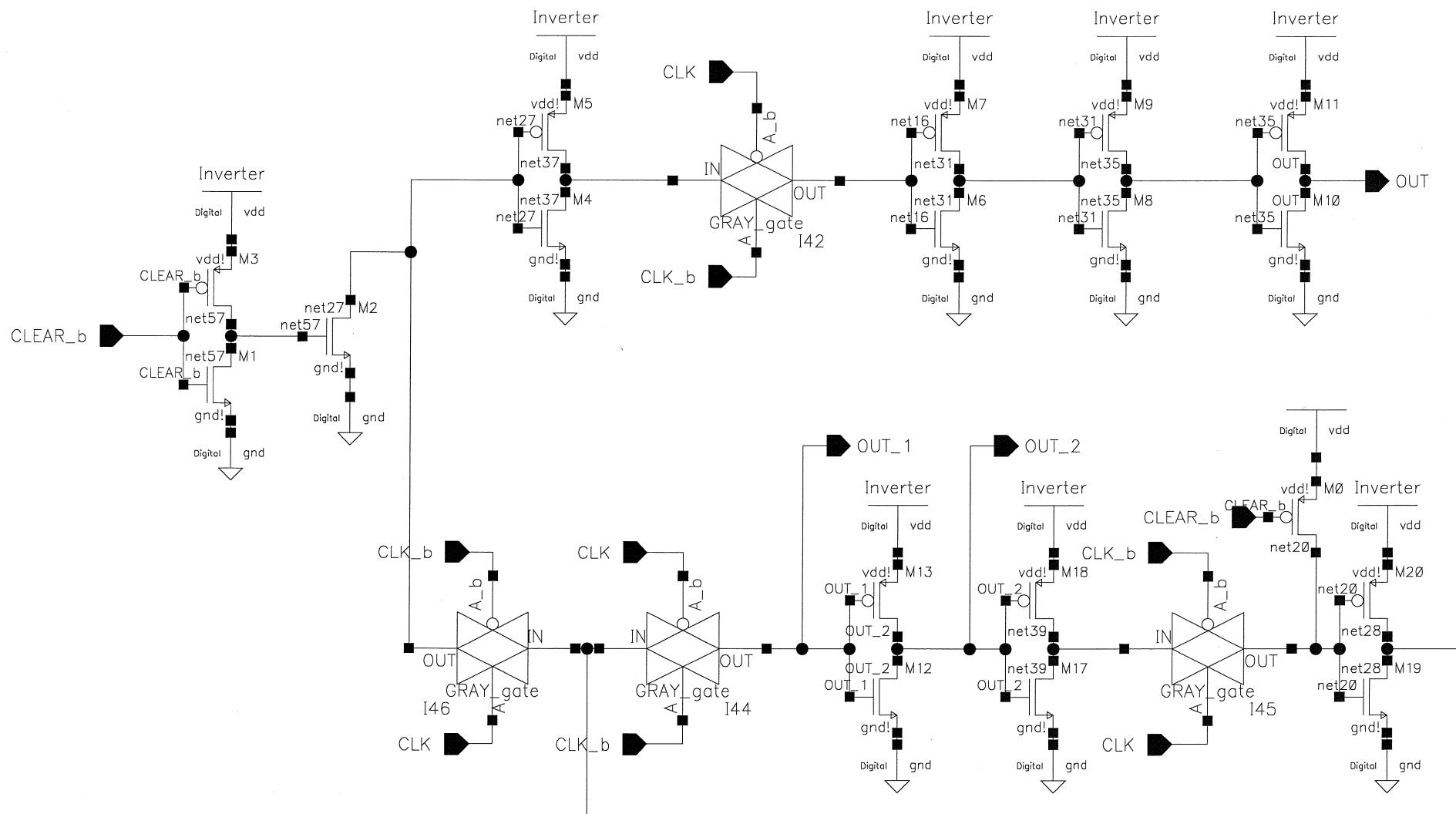
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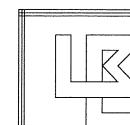
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This circuit starts off the GRAY COUNTER



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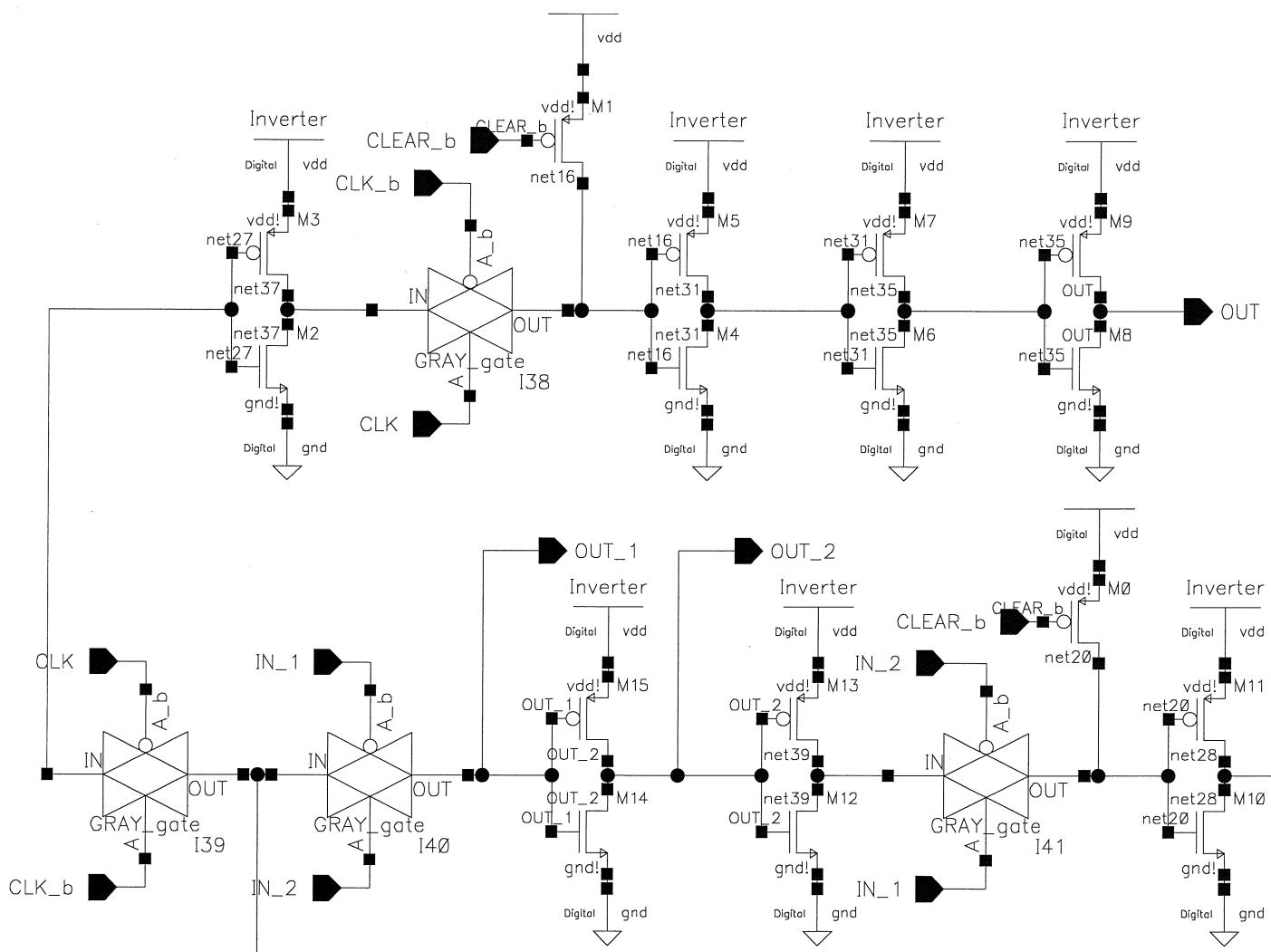
Library: OATWD

CellName: GRAY_Start

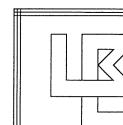
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This is one of the middle bits of the GREY_COUNTER



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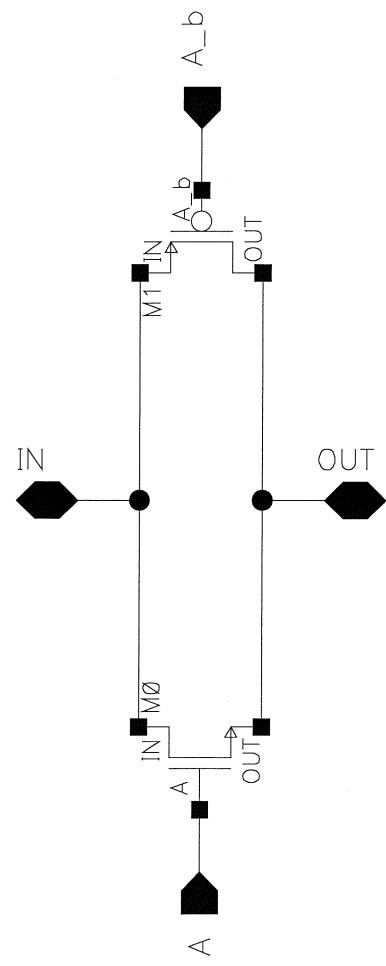
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CellName: GRAY_Bit

UPDATE: Sep 28 16:37:17 1999

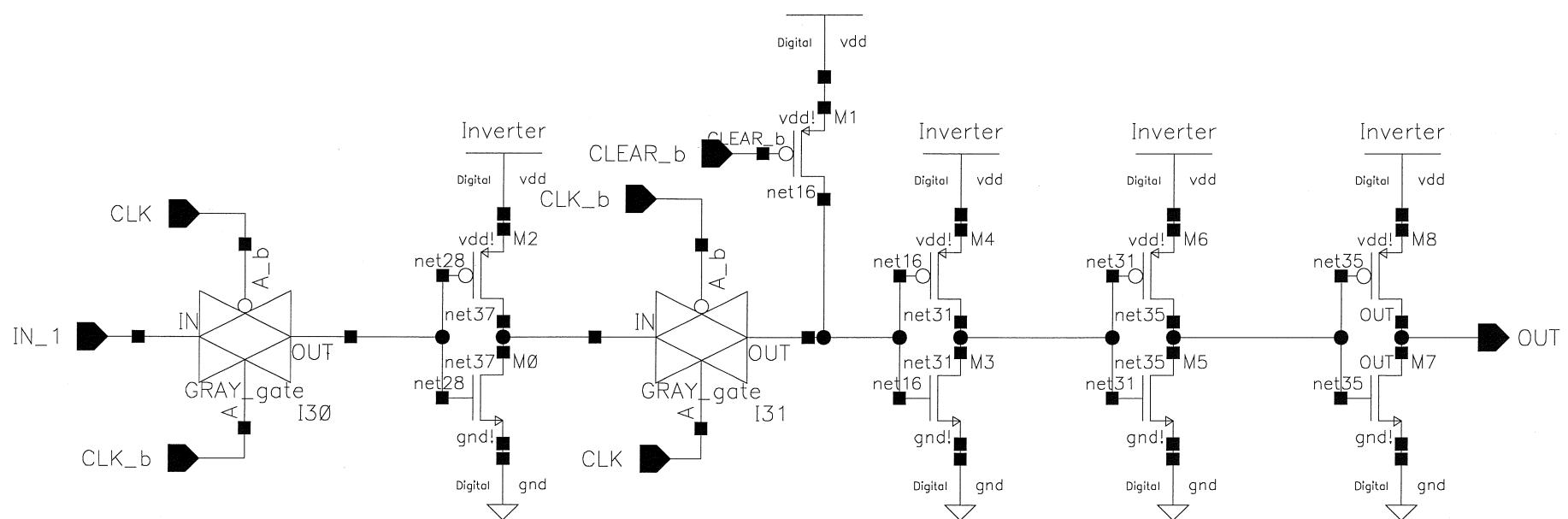
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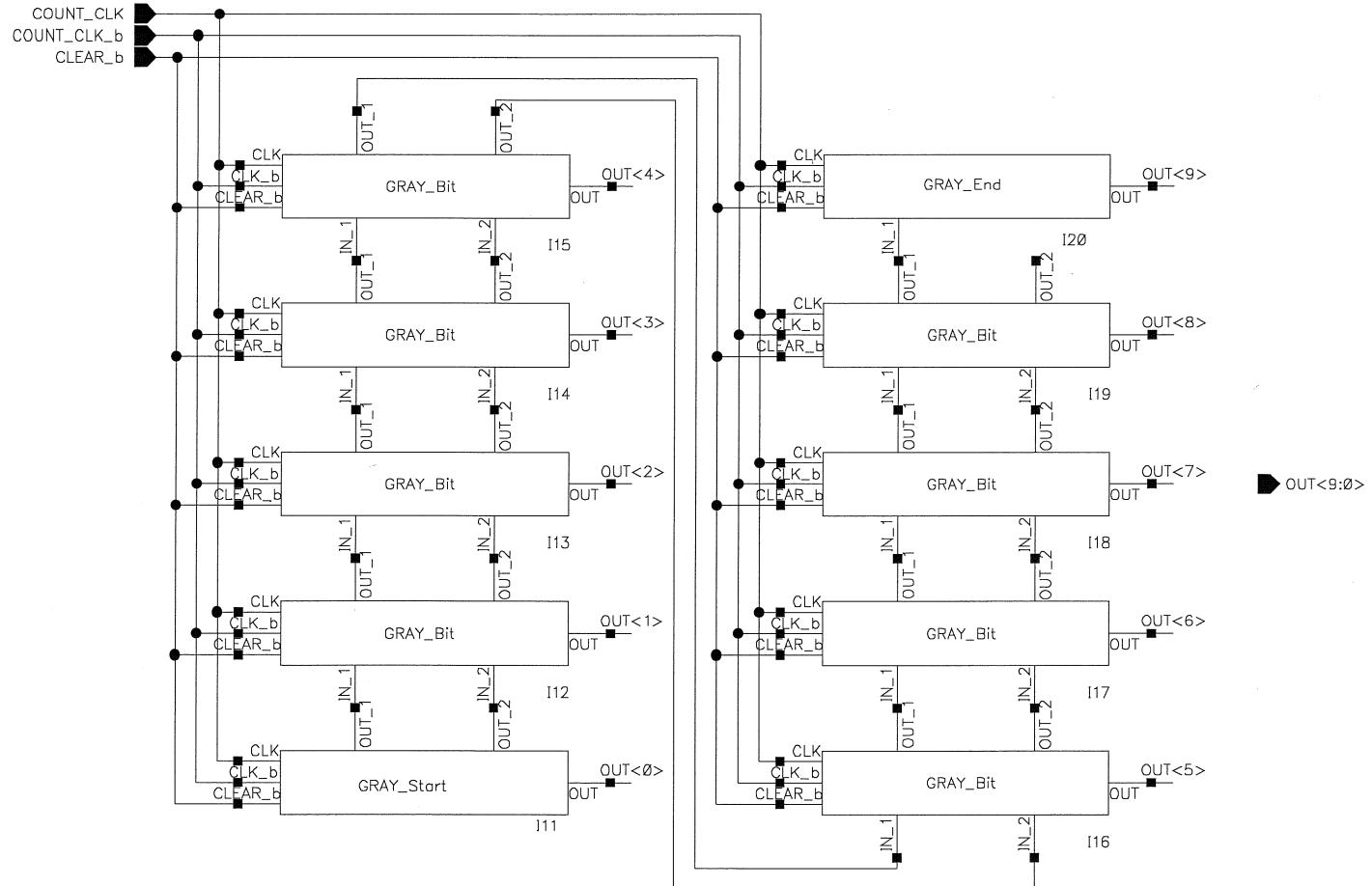
This is the transmission gate for the digital logic
in the GREY_COUNTER.

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	Project: Analog Transient Waveform Digitizer
Library:	OATWD
CellName:	GRAY_gate
UPDATE:	Sep 28 16:37:15 1999
DESIGN:	oren
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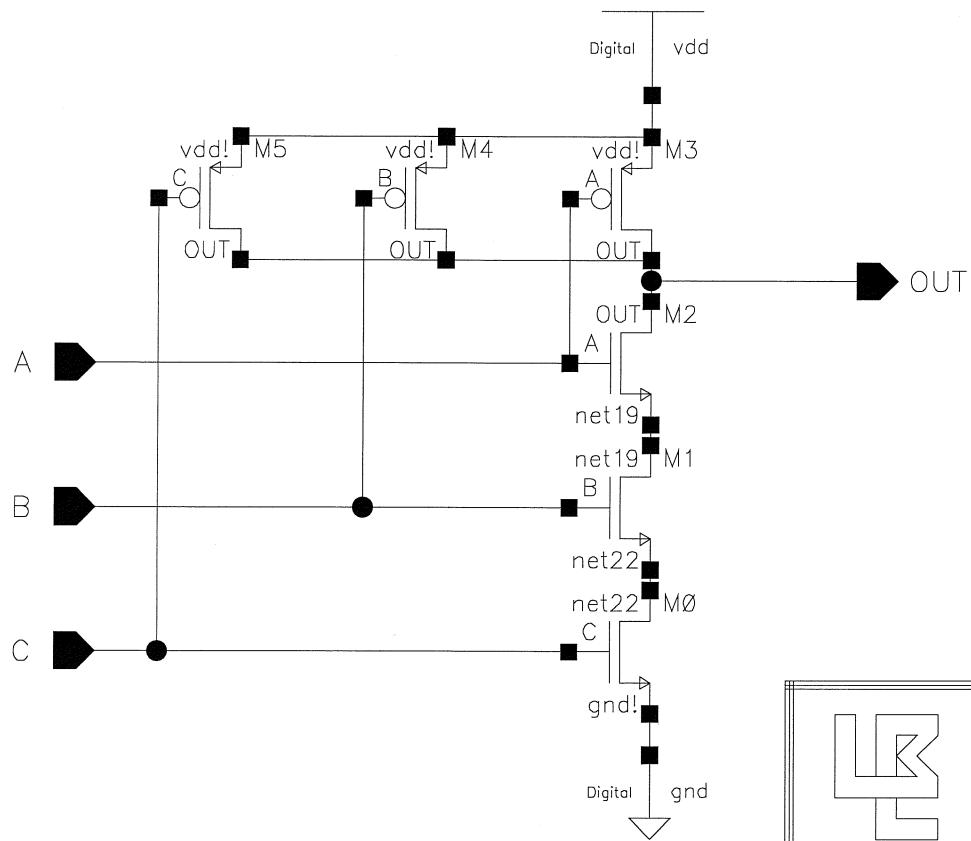
This is the last bit in the GRAY COUNTER.

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	Project: Analog Transient Waveform Digitizer
Library:	OATWD
CellName:	GRAY_End
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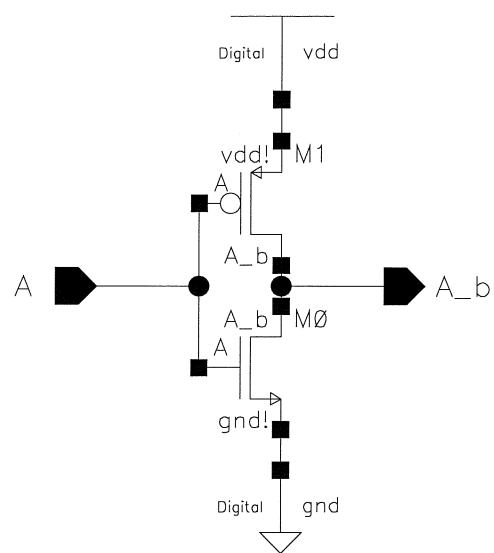
The Grey Counter cycles through 1024 (2^{10}) grey digits. The counter changes on the rise AND fall of the COUNT_CLK.

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	Project: Analog Transient Waveform Digitizer
Library:	OATWD
CellName:	GRAY_COUNTER
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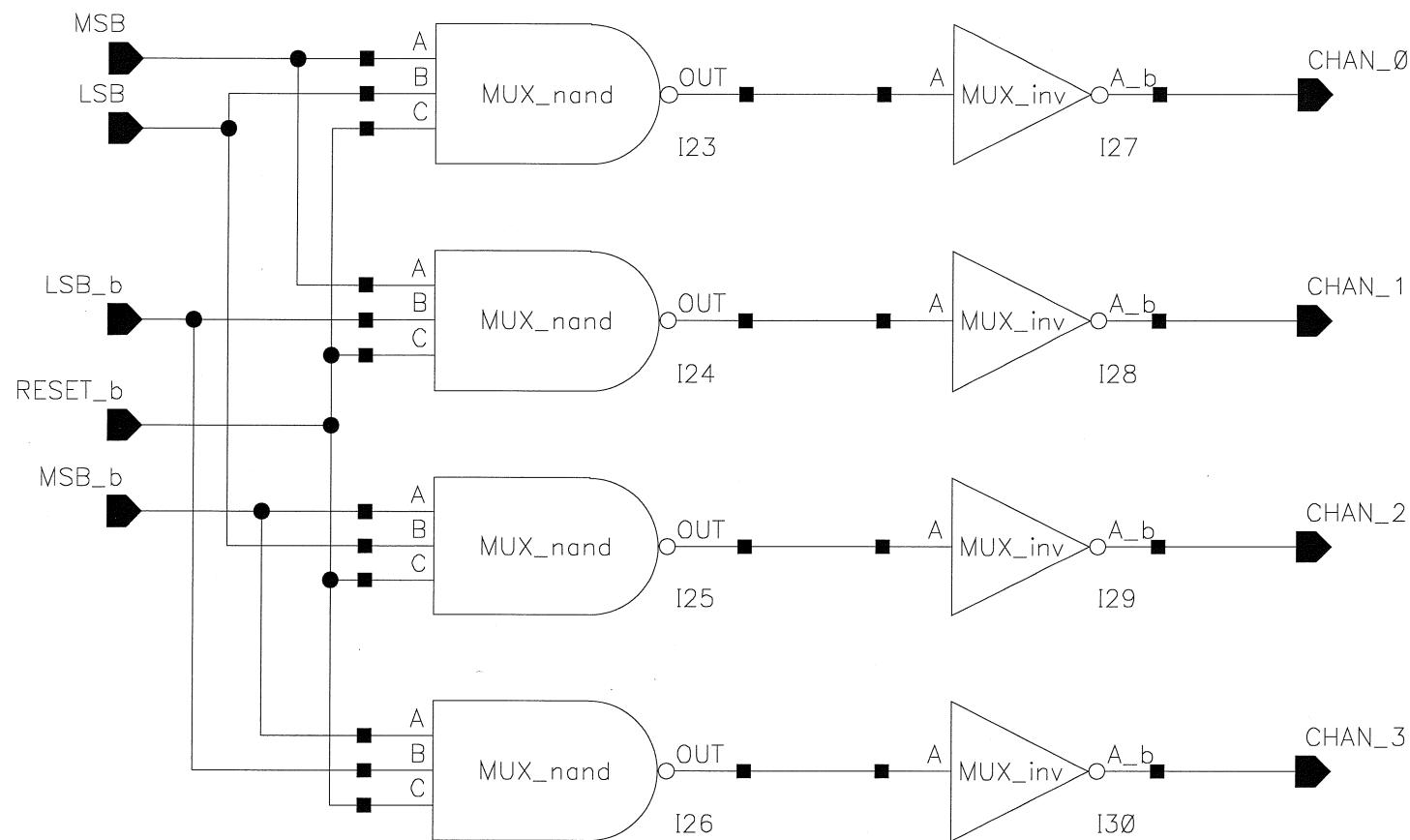
A trigate NAND gate for the MUX circuit

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	Project: Analog Transient Waveform Digitizer
Library:	OATWD
CellName:	MUX_nand
UPDATE:	Sep 28 16:37:14 1999
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This inverter is for the MUX circuit

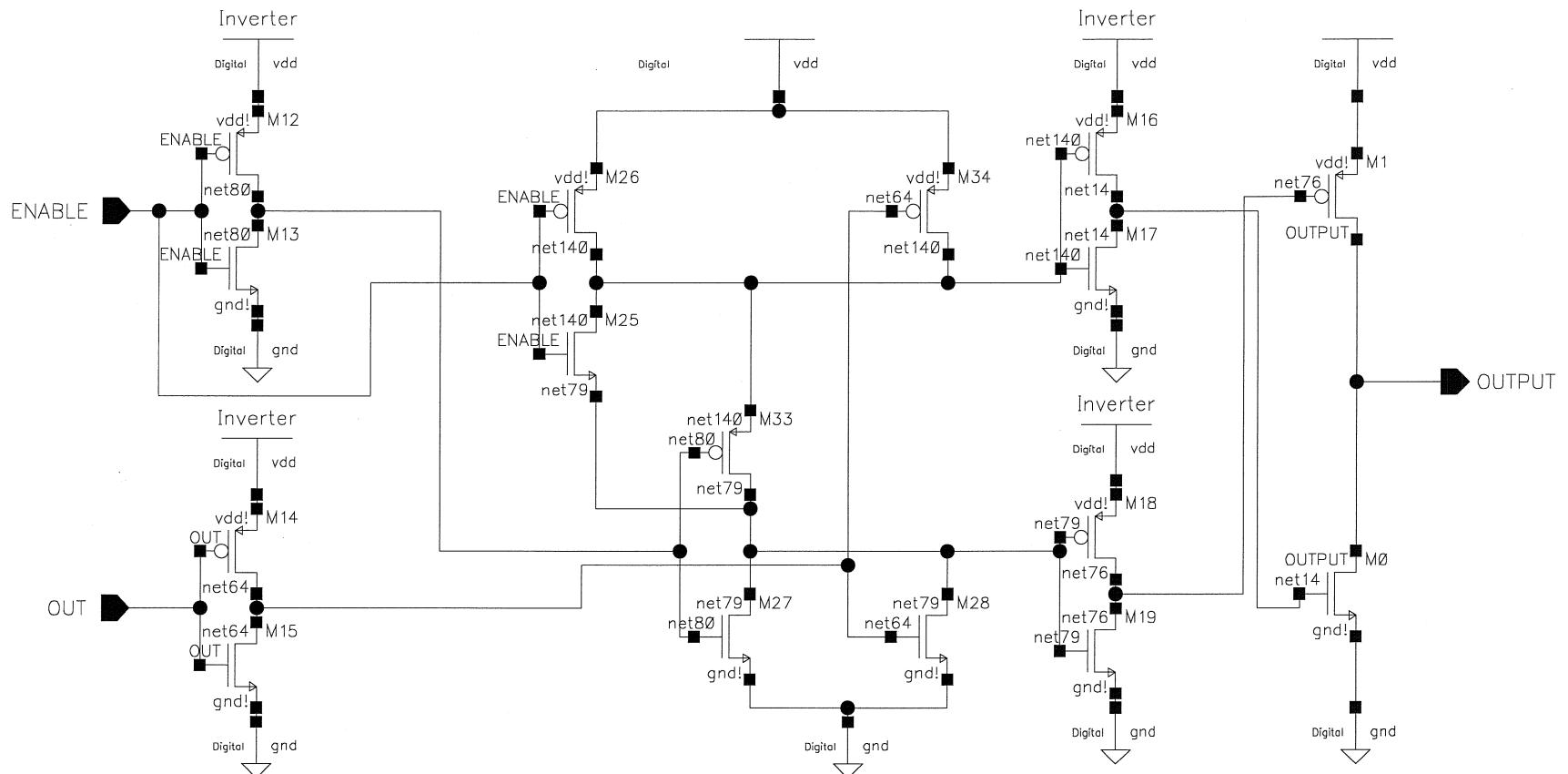
	Lawrence Berkeley National Lab
	Project: Analog Transient Waveform Digitizer
Library:	OATWD
CellName:	MUX_inv
UPDATE:	Sep 28 16:37:13 1999
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This MUX decodes the 2-bit code for the Channel Selector into four separate signals.

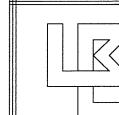
Note: RESET_b must be high to select a channel. This insures that the OP-AMP will not be shorted while the digitization is taking place.

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	Project: Analog Transient Waveform Digitizer
Library:	OATWD
CellName:	MUX
UPDATE:	Sep 28 16:37:14 1999
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This digital out is not active unless the enable bit is also set.

OUTPUT when ENABLE is low: 2.5 V.
OUTPUT when ENABLE is high: LOW = 10 uV. HIGH = 5 V.



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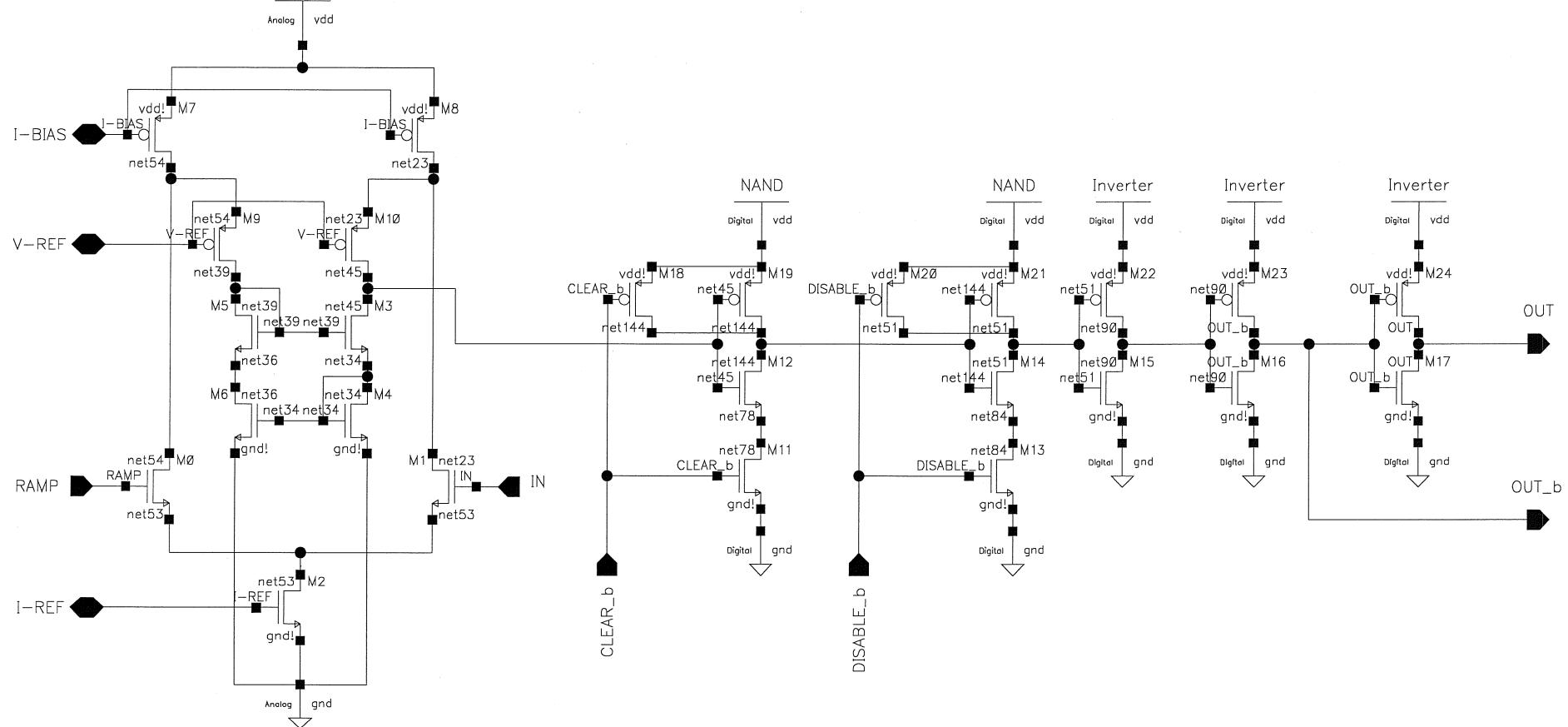
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CellName: OUT

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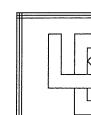
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The comparator compares two different voltages. When the RAMP voltage is higher than the COMP_IN voltage, the output from the comparator is high. That signal is passed on to two nand gates that act like inverters when CLEAR_b and DISABLE_b are asserted. Then it goes through three more inverters.

Bottomline: When RAMP is higher than COMP_IN, OUT is low. When RAMP is lower than COMP_IN, OUT is high.



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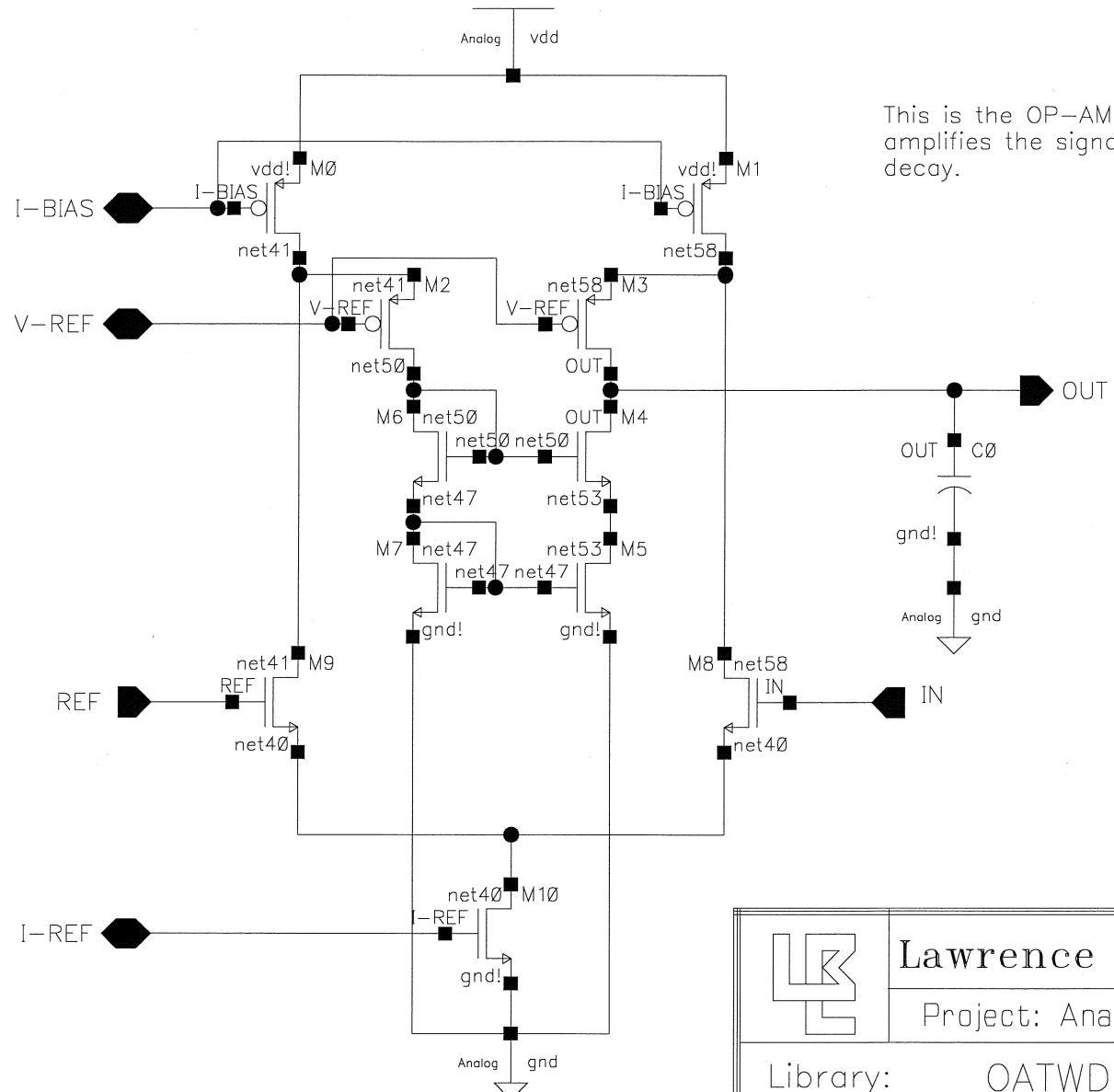
Library: OATWD

CellName: COMP

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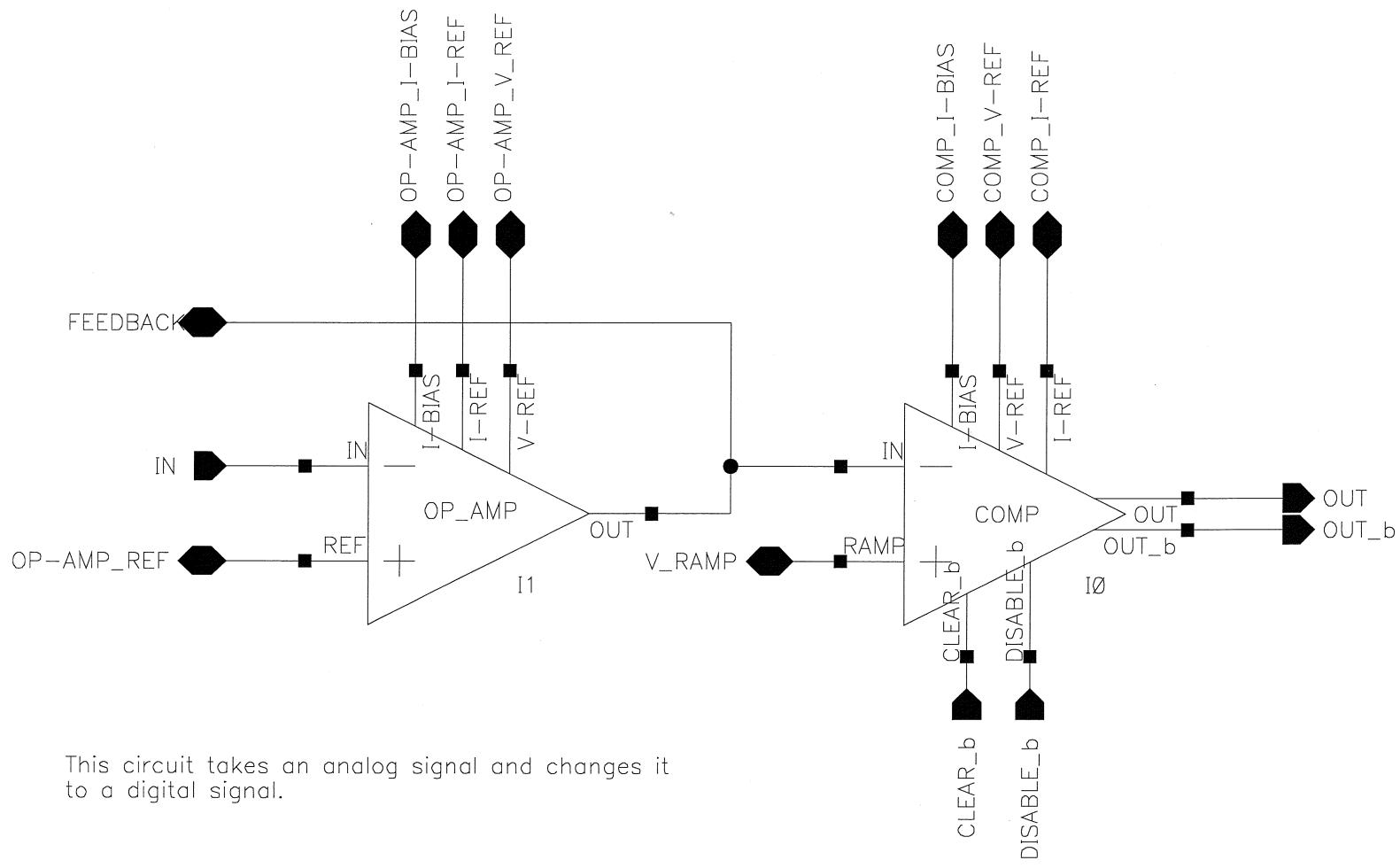
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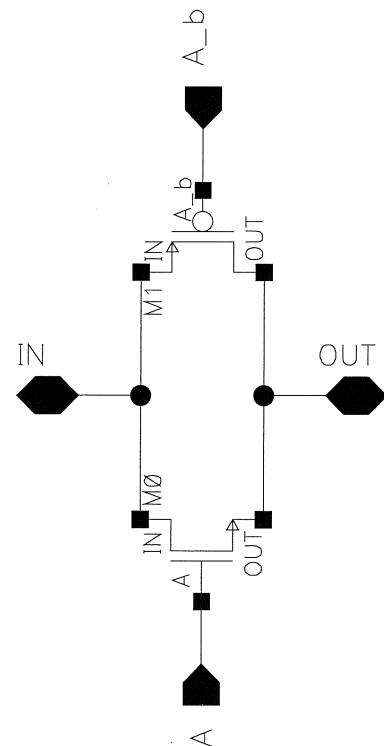


This is the OP-AMP for the digitization process. It amplifies the signal from the CAPS so that it doesn't decay.

	Lawrence Berkeley National Lab
	Project: Analog Transient Waveform Digitizer
Library:	OATWD
CellName:	OP_AMP
UPDATE:	Sep 28 16:37:10 1999
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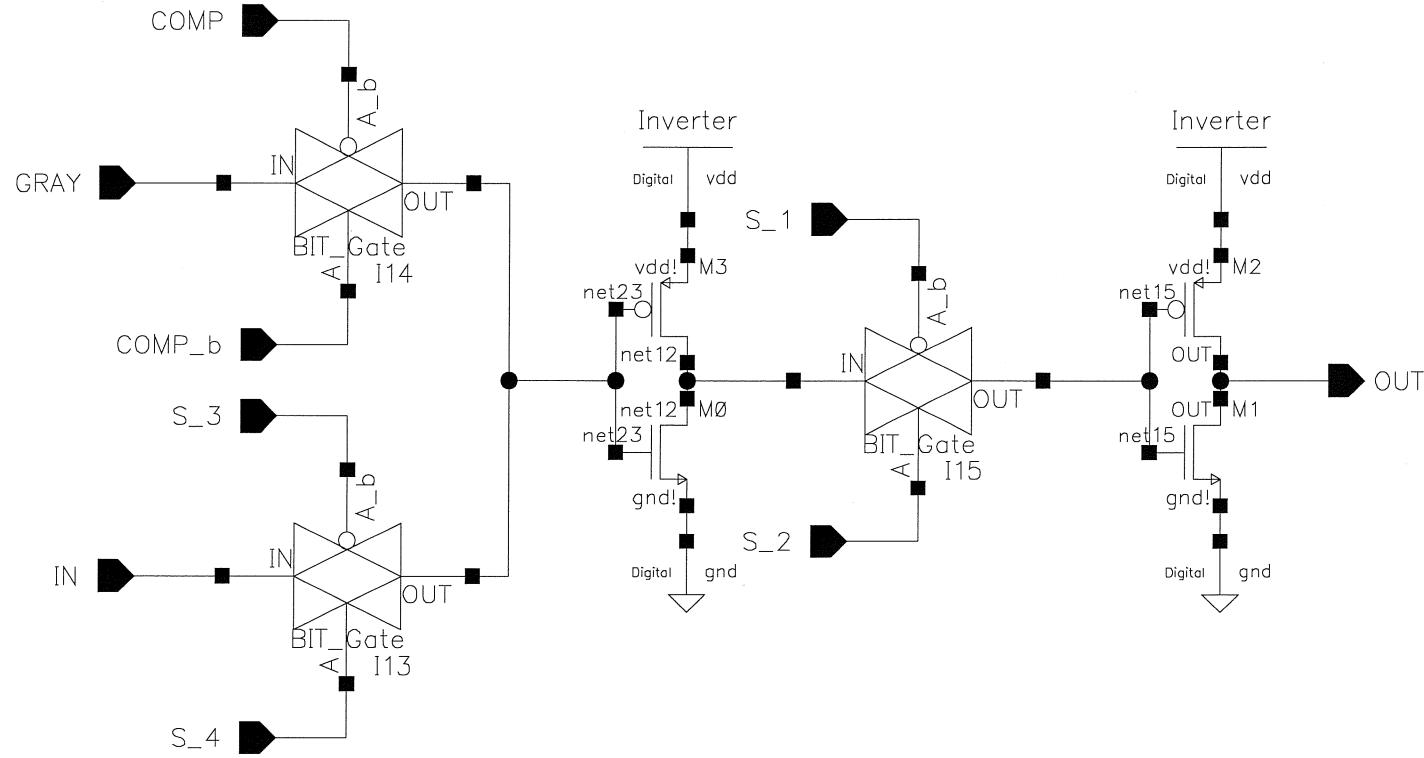


	Lawrence Berkeley National Lab
	Project: Analog Transient Waveform Digitizer
Library:	OATWD
CellName:	CONVERTER
UPDATE:	Sep 28 16:37:11 1999
DESIGN:	oren
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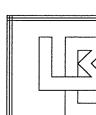
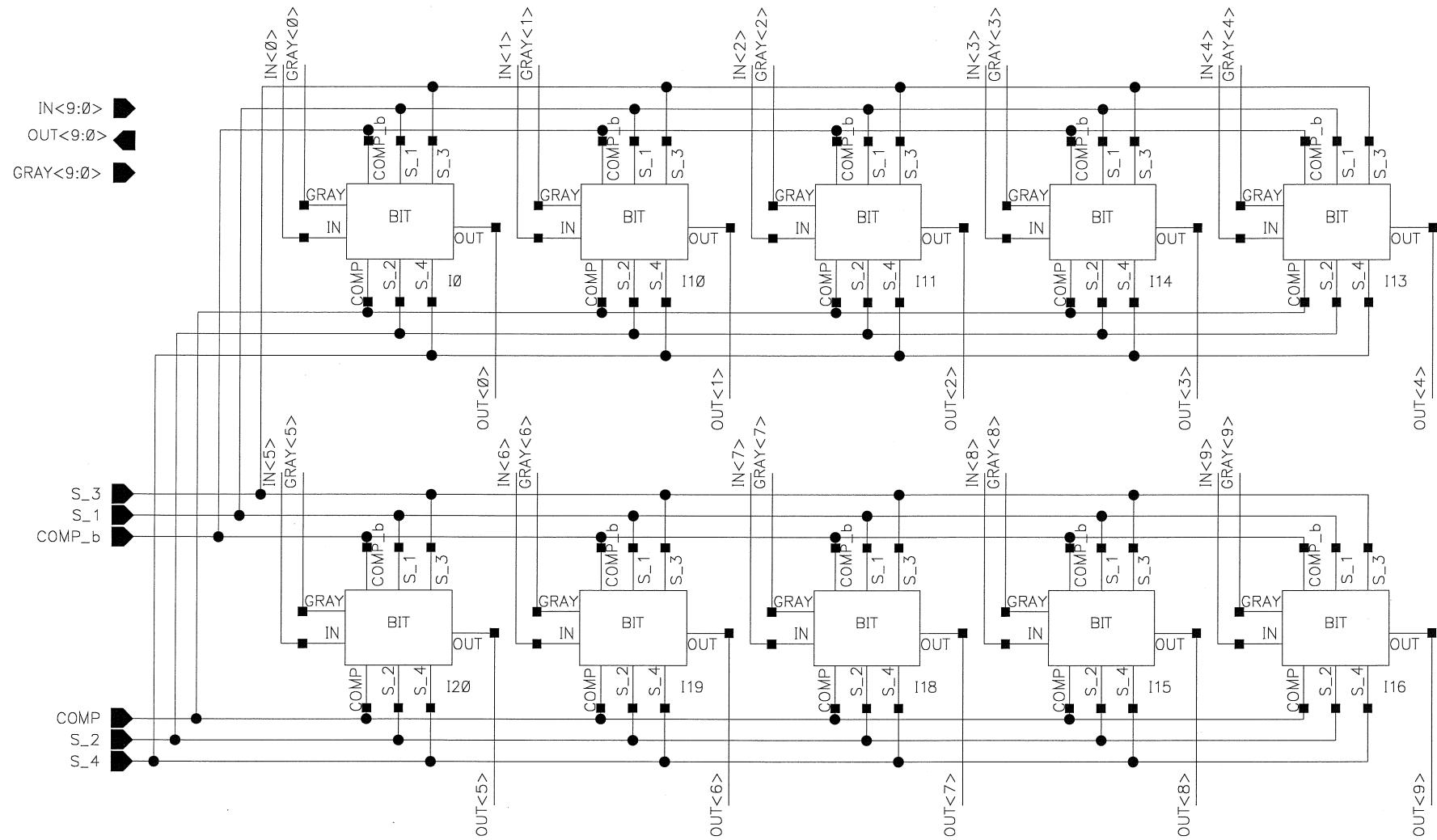
This is the transmission gate for the digital logic in the BITS.

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	Project: Analog Transient Waveform Digitizer
Library:	OATWD
CellName:	BIT_Gate
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The BIT is a circuit is a latch and a shifter. When the V-RAMP value decreases past the V-IN value, the COMP_b latch closes, storing the value of the GRAY_CODE. This value is then shifted out by the SHIFT_CLOCK. The SHIFT_CLOCK shifts the value from IN to OUT.

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	Project: Analog Transient Waveform Digitizer	
Library:	OATWD	
CellName:	BIT	
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Project: Analog Transient Waveform Digitizer

Library: OATWD

CellName: SHIFT_LATCH

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